

≈ 1970

The Model 4

A total approach
to General Purpose
Computing

 **INTERDATA®**

Introduction to the Model 4

The INTERDATA Model 4 is a significant departure from the conventional structure of the small computer. The Model 4 represents the latest advances in 3rd generation concepts to provide you with the powerful features of larger computers, at small computer prices.

Features like:

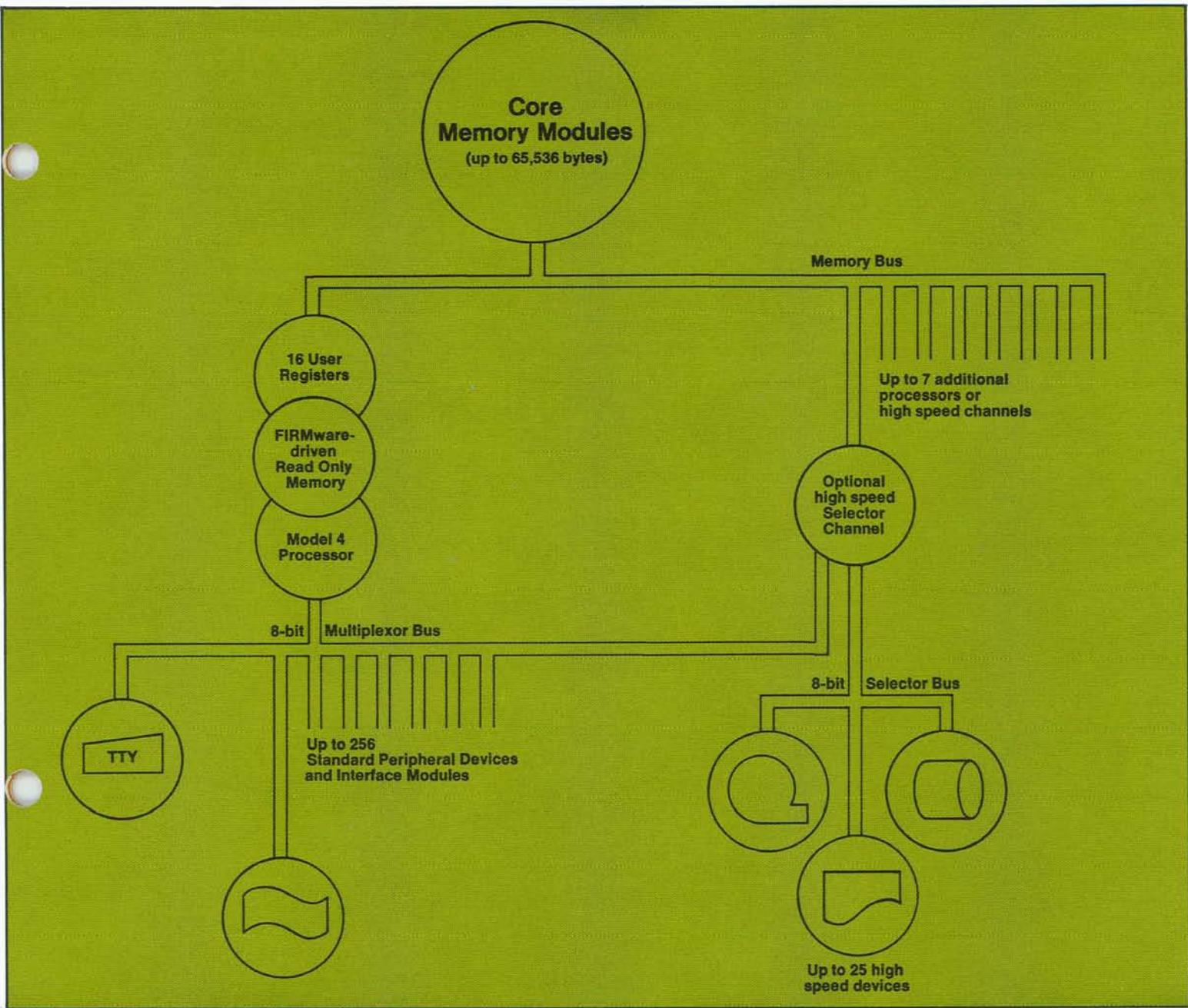
- 16 hardware general registers
- 1 microsecond core memory cycle time
- up to 65K bytes of memory — directly addressable
- 75 basic instructions
- 15 hardware index registers.
- extensive software library
- a sophisticated I/O structure
- a complete line of peripherals

Feature	Typical 2nd Gen. Computers	3rd Gen. Computer
Register	1 accumulator 1 index register	16 accumulators, 15 of these can be as index registers
Instruction Sets	small — often only 8-16 basic	75 basic instructions
Instructions Options	limited usually to multiply/divide	expandable through FIRMWARE
Addressing	limited capacity requires "paging" or "sectorizing"	direct addressing of up to 65,536 bytes eliminates paging
Word length	Fixed	multiple: 8, 16 and 32 bit
I/O Structure	uses software "polling techniques"	Automatic hardware interrupting device identification and status monitoring

Architecture

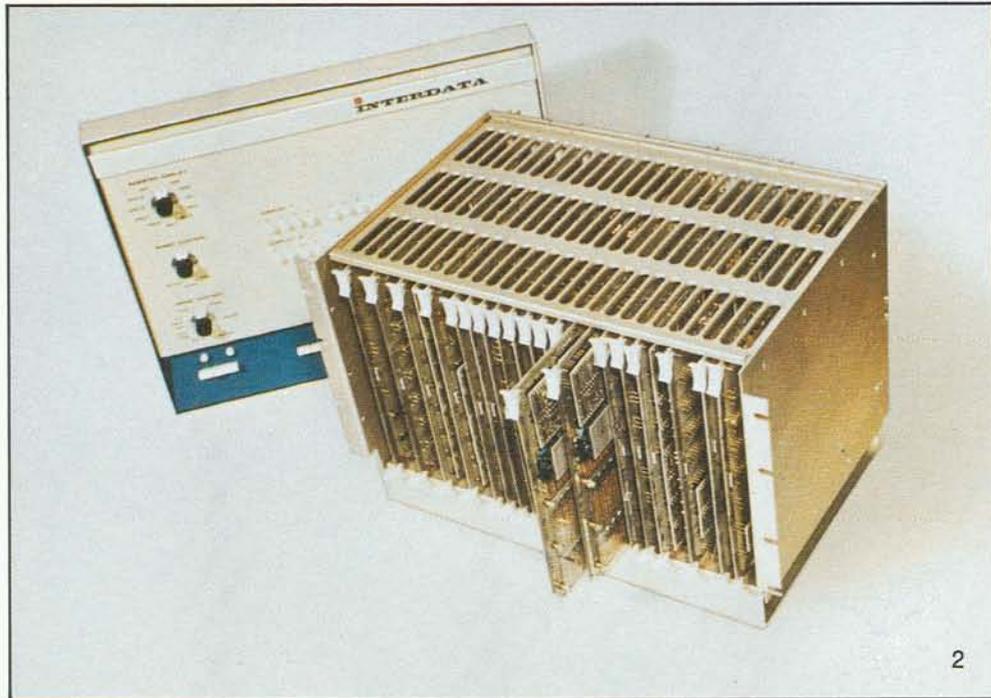
The INTERDATA Model 4 is modularly structured to provide a high degree of flexibility in configuring application-oriented systems. Up to 8 processors, High

Speed Memory Bus Interfaces, or Selector Channels may be connected to the Memory Bus. Memory is field expandable to 65K bytes — requiring only plug-in of additional modules to a pre-wired chassis.



Interdata digital systems are modularly structured to provide a high degree of flexibility in configuring application-oriented systems. The "building blocks" are all expandable to allow the system to grow with its user's needs. A combination of up to 8 processors, Selector Channels or Direct Memory Access Channels may be connected to the Memory Bus. Field Expansion of memory requires only plug-in of additional modules to a pre-wired chassis. The memory modules of most Interdata systems can be expanded to a maximum direct addressing range of 65,536 bytes.

Shown at right is a basic Model 4 central processor with 8K bytes of memory and I/O slots for three peripheral devices.



FIRMWARE

The FIRMWARE concept, pioneered by INTERDATA, is a technique whereby a microcoded "inner processor" functions as the control mechanism of the main computer. Operating at 400 nanoseconds per cycle, FIRMWARE directs register manipulations and data transfers within the computer.

The FIRMWARE program is hardwired into a permanent nondestructible read-only-memory (ROM), resulting in a highly versatile machine which offers an impressive price performance ratio.

FIRMWARE Support INTERDATA provides the Model 4 with software packages allowing the user to assemble and simulate his microcoded program very much the same as a software program.

FIRMWARE Assemblers These programs accept source tapes for micro-programs and generate ROM object tapes. With these assemblers, micro-operation codes have symbolic names, operands have symbolic names, numbers can be written in a natural way, locations have symbolic names, and error checking is performed. These assemblers run on any standard INTERDATA system with 8K bytes of memory and a teletype.

Simulators The simulators are used for testing and debugging micro-programs before they are wired into a ROM. The simulators

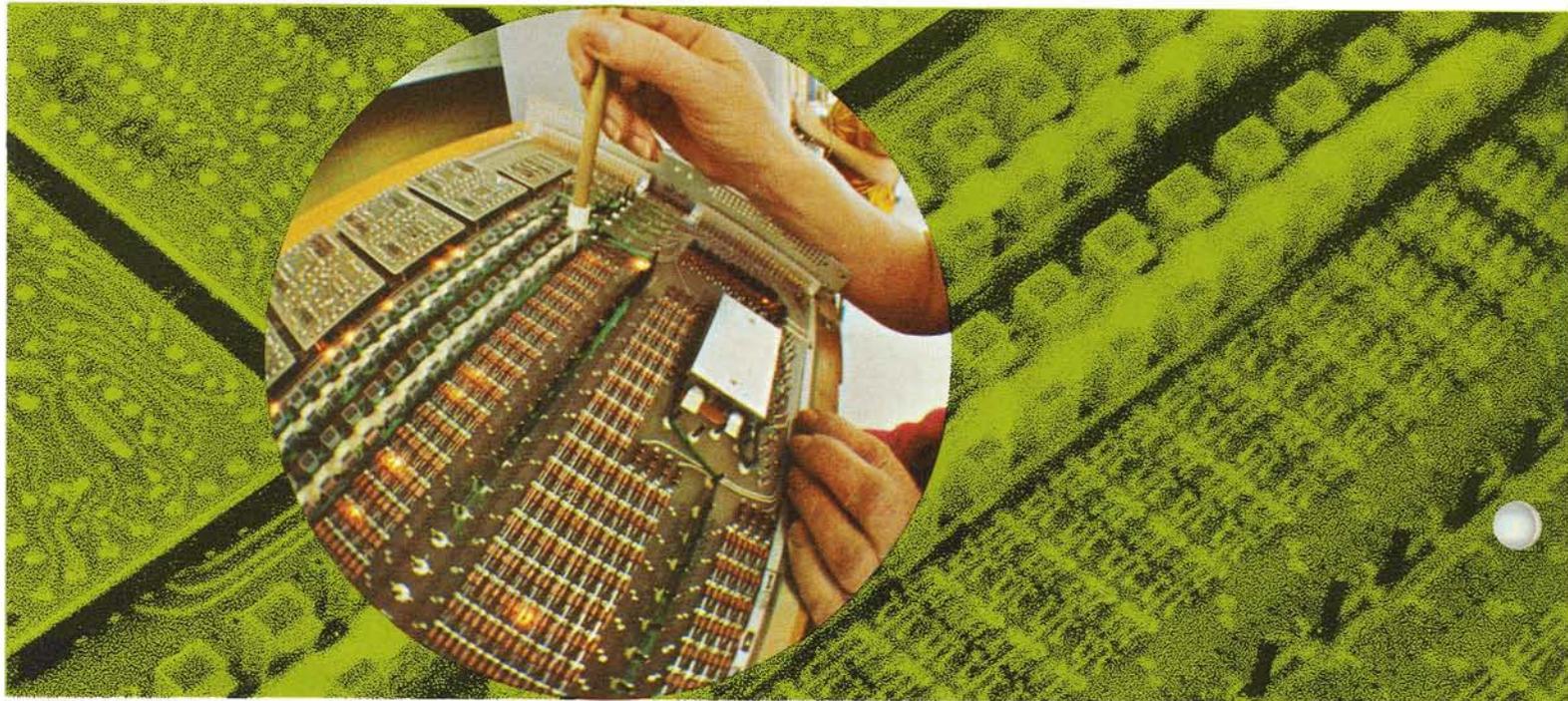
are interactive and allow the debugging process to proceed under teletype control with continuous observation by the designer. The simulators will read ROM object tapes, execute the micro-programs, and punch a corrected ROM object tape. 8k bytes of memory are required.

The result is a customized computer tailored to the individual users needs, while preserving the software features of a general purpose machine.

FIRMWARE Options The versatility and programming power of the Model 4 is further enhanced by a wide array of application oriented FIRMWARE optional packages. These packages are offered as plug-in or replacement read-only-memory modules. Field expansion is possible in most instances.

FIRMWARE packages available are:

1. High Speed Option
2. Fullword Instruction Set
3. Floating Point Expansion
4. Floating Point Trigonometric Expansion
5. Text Editing
6. Memory Accumulator Instruction Set
7. Indirect Instruction Set
8. Push down Table Manipulating Set



Software

INTERDATA's library of software packages has been designed to take advantage of the programming ease and power of the Model 4. This library includes: Fortran IV, Assembler, Real-Time Executive, On-line interactive debugging, Text Editor, extensive math library and I/O systems packages.

Fortran IV The Fortran IV Compiler for INTERDATA Digital Systems allows users to generate machine language programs using a problem-oriented language. The Fortran language is USASI Fortran IV, tailored to the real-time environment. Language features for manipulating interrupts and handling real-time input/output are provided. Assembly language statements and Fortran statements can be intermixed. The compiler provides extensive diagnostics during compilation to assist the user. The Fortran compiler requires 16K bytes of memory and operates under the INTERDATA Executive Systems. The generated object code is relocatable.

Program Preparation on Other Computers INTERDATA customers have access to assemblers and compilers which operate on larger general purpose computers or on time sharing networks. A basic assembler, written in Fortran IV, and

an expanded assembler, written in PL1, are available. An assembler and simulator for INTERDATA systems are currently running on several time sharing systems.

Executive — The Basic Executive is designated to operate on a Model 4 with 8K bytes of core memory plus one teletype for operator communication and user I/O. The system loads and initiates program execution under operator control. It performs logical I/O for all standard peripherals — Teletype, Card Reader, Magnetic Tape, etc. I/O handlers are modular and can be included as required by each installation. The basic executive expands to include the capability of loading and executing programs from libraries residing on mass storage devices.

The Real-Time Executive, which requires 16K bytes, a real-time clock, and memory protect, provides all of the capabilities of a basic executive. It adds ability of scheduling the execution of programs based on a real-time clock and real-time events. The system handles re-entrant real-time foreground programs plus background processing. The addition of mass storage enables the system to handle nonresident foreground programs.

Debugging An on-line interactive program allows examination and

modification of core memory in hexadecimal notation. Bias handling is provided for referencing and displaying relocatable programs. Object tapes can be generated for any block of memory in either 8-bit or standard binary tape formats. Symbolic disassembly of programs from core memory is provided.

Features available to the user are:

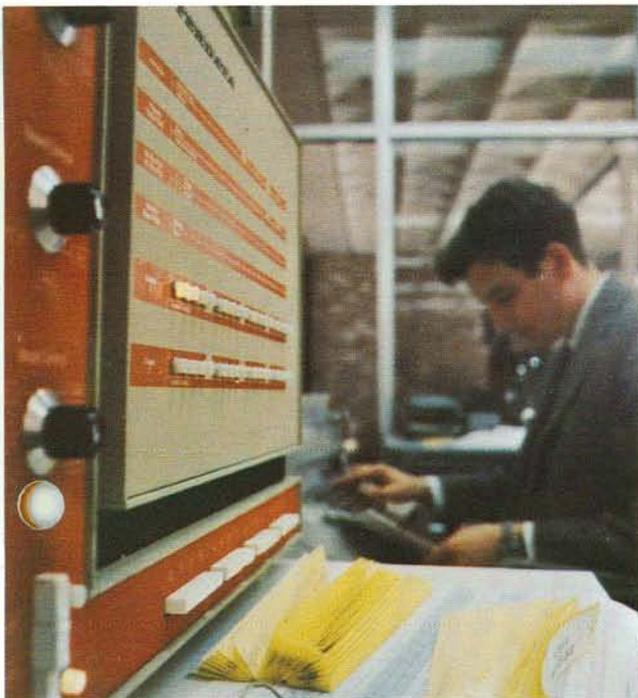
- Examine and modify a memory cell
- Address arithmetic
- Relative addressing of memory
- Multiple break points
- Search on limits for masked value
- Print or punch content of memory
- Execute the user programs
- Register examination

Editor An on-line interactive text editor allows direct entry of source statements into memory. These statements can be freely listed, changed, deleted, or augmented while remaining in core memory. Edited statements can then be output to form a source tape.

Math Library A complete math library of function routines in fixed and floating point is provided with INTERDATA systems.

Input/Output The input/output system provides driver packages for peripheral devices and system modules in addition to media conversion utility routines.

Model 3 and Model 4 multiprocessor systems for a multi-task control application.



Instruction Repertoire

A simple instruction repertoire may mean months of struggling for your programmers . . . a powerful instruction repertoire will not only make their task much easier but, combined with multiple registers, and other 3rd generation features, will dramatically improve the real time performance of the system.

What comprises a powerful instruction repertoire? One manufacturer lists 75 instructions when, in effect, his processor provides only 8 basic functions. Many of the others use the same tactics by listing dozens of trivial combinations.

The INTERDATA instruction set has 55-57 basic instructions plus options. They operate at highly effective speeds due to 3rd generation architecture; they are purposely designed for real time scientific and industrial applications.

Third Generation Instruction Format

Register to Register format: RR

0	7	8	11	12	15
OP	R1		R2		

Register to Indexed Memory format: RX

0	7	8	11	12	15	16	31
OP	R1	X2		Address			

Register to Indexed Data format: RS

0	7	8	11	12	15	16	31
OP	R1	X2		Data			

Program Status Word

0	11	12	15	16	31
Status		Condition Code		Instruction Address	

The system has three instruction formats. The 16-bit halfword instructions are the RR format. The 32-bit fullword instructions are the RX and RS formats.

The 4-bit R1, R2 (and X2) fields each specify one of the sixteen general registers. Each of the 16 halfword general registers can be used as a fixed point arithmetic accumulator or as a logical accumulator. Fifteen of the 16 general registers can be used as index registers.

The RR instructions are for operations between the general registers. The R1 and R2 fields specify the first and second operands respectively. For a register-to-register Add operation $[(R1) + (R2) \rightarrow (R1)]$.

The RX instructions are for operations between the general registers and memory. The R1 field specifies the first operand and the sum of the X2 and Address field specify the address of the second operand. For a register-to-indexed memory Add operation $[(R1) + (Address + X2) \rightarrow (R1)]$.

Immediate instructions RS are included for shifting and branching. Operations involving immediate operands also use the RX format. For the immediate instruction the R1 field specifies the first operand and the sum of the contents of the X2 and Address field form the second operand. For an Add immediate operation $[(R1) + Address + (X2) \rightarrow (R1)]$. The shift count is given by $[Address + (X2)]$.

Instruction alignment — Halfword RR format instructions and fullword RX and RS format instructions are aligned on halfword boundaries. This permits mixing of halfword and fullword instructions with no requirement for halfword NO-OP's to force correct fullword instruction memory alignment.

Program Status Word — The status of the machine is defined by the program status word. It contains the Status, Condition Code and Instruction Address.



Instruction Repertoire

Type	Instruction	Mnemonic	
Load and Store Instructions	Load Halfword	LHR	
	Load Halfword	LH	
	Load Halfword Immediate	LHI	
	Store Halfword	STH	
	Load Byte	LBR	
		LB	
	Store Byte	STBR	
		STB	
	Load Program Status Word	LPSW	
	Unchain	UNCH	
Fixed Point Arithmetic Instructions	Load Multiple	LM	
	Store Multiple	STM	
	Autoload	AL	
	Add	AHR	
		AH	
		AHI	
	Add with Carry Halfword	ACHR	
		ACH	
	Subtract Halfword	SHR	
		SH	
	SHI		
	SCHR		
	SCH		
Logical Instructions	AND Halfword	NHR	
		NH	
		NHI	
	Inclusive OR Halfword	OHR	
		OH	
		OHI	
	Exclusive OR Halfword	XHR	
		XH	
		XHI	
		CLHR	
	CLH		
	CLHI		
Input output Instructions	Read Data	RDR	
		RD	
	Write Data	WDR	
		WD	
	*Read Block (optional)	RBR	
		RB	
	*Write Block (optional)	WBR	
		WB	
	Device Interrupt Control Instructions	Acknowledge Interrupt	AIR
			AI
Sense Status		SSR	
		SS	
Output Command		OCR	
		OC	
Shift Instructions		Shift Left Arithmetic	SLHA
		Shift Right Arithmetic	SRHA
		Shift Left Logical	SLHL
		Shift Right Logical	SRHL
Branch Instructions	Branch AND Link	BALR	
		BAL	
	Branch on False Condition	BFCR	
		BFC	
	Branch on True Condition	BTCR	
		BTC	
	Branch on Index Low or Equal	BXLE	
	Branch on Index High	BXH	
	Branch Unconditional	BR	
		B	
Extended Mnemonics	Branch on Zero	BZ	
	Branch on Not Zero	BNZ	
	Branch on Plus	BP	
	Branch on Not Plus	BNP	
	Branch on Minus	BM	

Type	Instruction	Mnemonic	
	Branch on Not Minus	BNM	
	Branch on Carry	BC	
	Branch on Overflow	BO	
	Branch on Low	BL	
	Branch on Not Low	BNL	
	Branch on Equal	BE	
	Branch on Not Equal	BNE	
	No Operation	NOPH	
		NOP	
	STANDARD OPTIONS		
Fixed Point Arithmetic Instructions	Multiply Halfword (optional)	MHR	
		MH	
	Divide Halfword (optional)	DHR	
		DH	
		AE	
		SE	
		ME	
		DE	
		LE	
		STE	
	CE		
Floating Point Arithmetic Instructions (optional)	Add	AE	
	Subtract	SE	
	Multiply	ME	
	Divide	DE	
	Load	LE	
	Store	STE	
	Compare	CE	
	Floating Point Trigonometric Instructions	Floating Point Square Root (RR)	SQER
		Floating Point Square Root	SQE
		Floating Point Sine	SINE
	Floating Point Cosine	COSE	
	Floating Point Arc Tangent	ACTE	
Fullword (32 bit) Fixed Point Instructions	Load Fullword	L	
	Store Fullword	ST	
	Add Fullword	A	
	Subtract Fullword	S	
	Compare Fullword	C	
	Shift Left Fullword Logical	SLL	
	Shift Right Fullword Logical	SRL	
	Rotate Left Fullword	RL	
	Rotate Right Fullword	RR	
	Compare Logical Byte (RR)	CLBR	
Text Editing Instructions	Compare Logical Byte	CLB	
	Translate (RR)	TRNR	
	Translate	TRN	
	Move (RR)	MOVR	
	Move	MOV	
	Find (RR)	FNDR	
	Find	FND	
	Advanced Programming Package Instructions	Load Indirect	LI
		Store Indirect	STI
		Branch on True Condition Indirect	BTCI
Branch on False Condition Indirect		BFCI	
Branch AND Link Indirect		BALI	
Add Halfword to Storage		AHS	
Subtract Halfword to Storage		SHS	
AND Halfword to Storage		NHS	
Inclusive OR Halfword to Storage		OHS	
Exclusive OR Halfword to Storage		XHS	
Special Instructions	Push	PHS	
	Pop	POP	
	Chain	CHN	
	Unchain	UNCH	
	Branch IF Multiplexor	BIM	
	Execute IF Multiplexor	EIR	
	Test Bit	TB	
	Set Bit	SB	
	Clear Bit	CB	

* Optional Firmware Instructions

I/O Structure

An I/O Structure which "unjams" the accumulator In most small computers, information coming from and going to the outside world passes through a single accumulator. This continuously requires instructions to unload and reload the previous computation. Not so with the INTERDATA Model 4. In the Model 4 structure, I/O transforms can be deposited in a spare accumulator within the 16 register stack WITHOUT affecting the previous computation. In addition, the data can be placed directly into memory — either under program control or over the optional cycle stealing ports such as the Selector Channel.

Automatic Hardware Polling with Simultaneous Device Status Many small computers require a considerable quantity of software processing to successfully interrogate devices to determine the interrupt source. The Model 4 structure embeds these housekeeping functions in hardware. The result is greater utilization of critical processor time.

I/O Control Concept The Model 4 I/O structure employs a highly reliable I/O request-response control mechanism. It is an automatic function which avoids "tricky" synchronization. This form of request-response takes no appreciable time and provides locked-in insurance against timing errors due to possible component degradation or environmental noise. As a result, interfacing problems are greatly simplified.

FIRMWARE enhances I/O Functions Special purpose FIRMWARE can be employed to further enhance real time I/O processing. At 400 nanosecond cycle speeds, FIRMWARE can perform extensive I/O control and data management. The resulting improvement in throughput can be from 3 to 10 times when compared to the performance of the same functions through software.

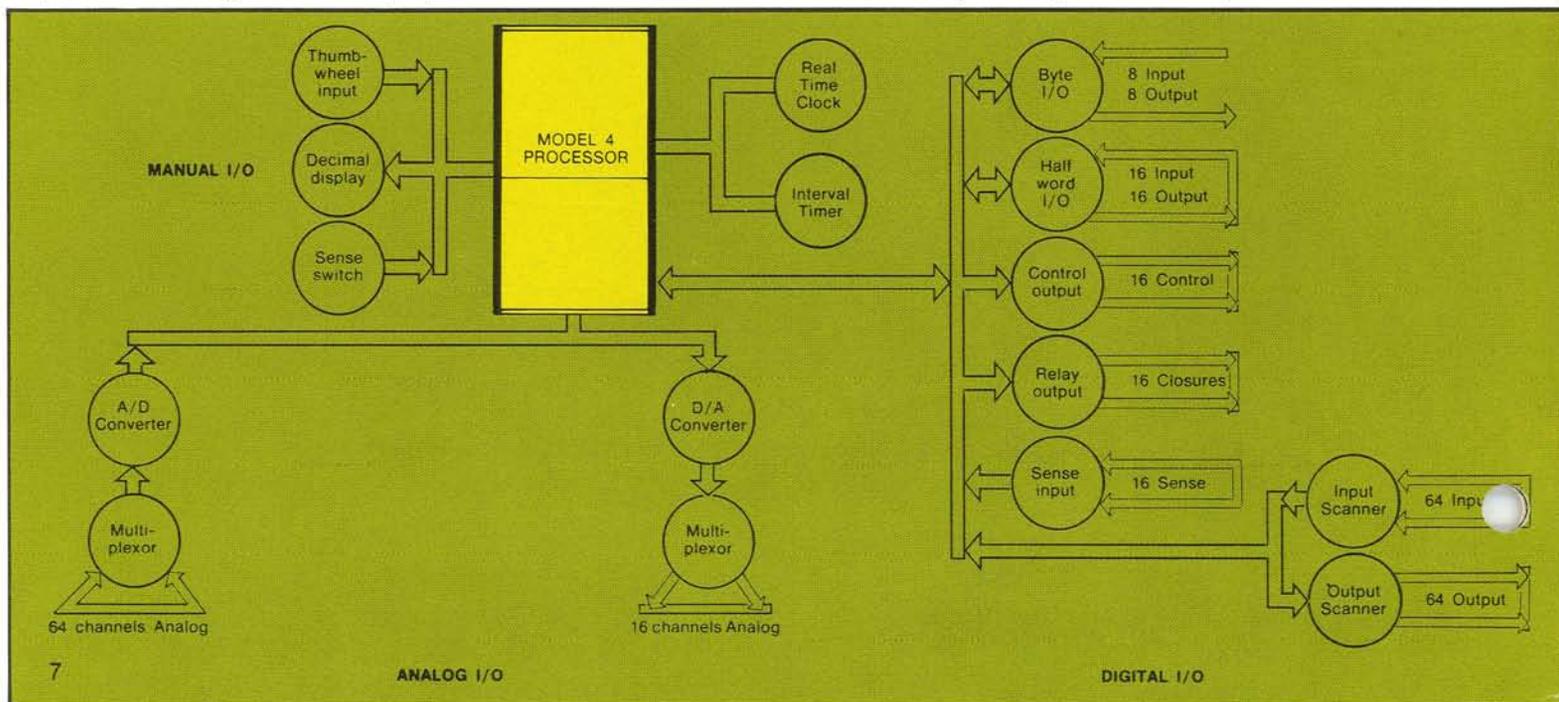
I/O Channels The 8-bit Model 4 Multiplexor Channel transfers byte oriented data under program control

between the processor and an active device. Either single bytes or a block of bytes can be transferred depending on the instruction used. Under program interrupt control a number of low speed devices can be operational at the same time. The interrupt organization permits the individual unique identification of up to 256 devices in a hardware priority structure with overriding enable/disable facilities. An optional 8-bit Selector Channel provides high speed, byte oriented data transfer between memory and an active device. The Selector Channel is initialized for block transfer by the processor, thereby freeing the processor for other work.

Standard Memory Bus Interface

The Standard Memory Bus Interface permits the user access to a 16 bit data word on a cycle stealing basis. This is provided as an optional system module for interfacing with customers special I/O devices.

System Modules to meet virtually all requirements. The success of a real-time system is based upon the efficiency of the Model 4 System Modularity. This concept permits the Model 4 to handle diverse analog and digital interface problems at minimal cost.



Peripheral Equipment

An outstanding line of field-proven peripheral equipment is available for the Model 4 system. These peripherals are designed to handle a wide range of user processing tasks.

The following peripheral equipment is available for the Model 4:

Teletype

ASR 33 — Available with a 10 cps read/punch/type speed
KSR 33, KSR 35, ASR 35 — Heavy duty types which complement the ASR 33 and the new ASR 37
GE Termi-Net 300 — Useful for higher speed applications

Paper Tape Equipment

A 300 cps reader and 60 cps punch are offered for the Model 4, individually, or as a complete package. Fan-fold tape is featured as the software media.

Card Reader

A 200 cpm reader is provided for card oriented input systems

Line Printer

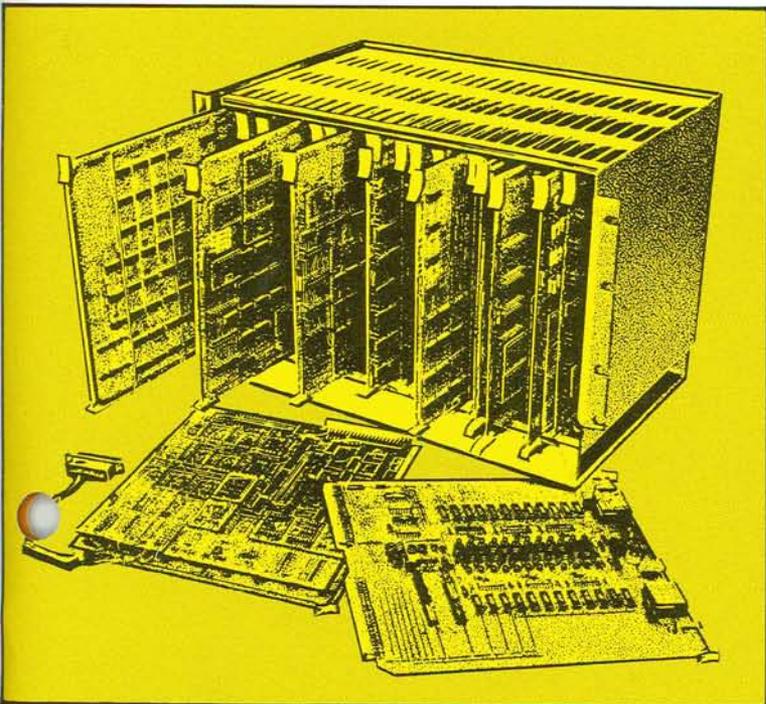
Provides 300 lpm capability with 132 columns per line and 64 characters. Ideally suited to fulfill your high speed listing requirements.

Bulk Storage

Fast access bulk storage media is offered in 131KB to 8.3MB sizes. Average transfer rates are 230KB/second with 8.7 and 17.4 microsecond average access times. IBM compatible seven and nine track tape transports are available for the Model 4 with 25 ips speed and densities of 556 bpi and 800 bpi.

Communication Devices

Line adapters for a broad spectrum of communication requirements are offered. Host computer interfaces for the IBM/360, Univac 1108, and Burroughs 5500 are also available for the Model 4. Data set adapters for Bell units include the 103, 201, 202, and 301 with various options.



Customer Support

With hundreds of installed computer systems, INTERDATA maintains an extensive program of customer support activities. You are encouraged to avail yourself of these services in order to effectively utilize the Model 4's capabilities.

Customer Training Hundreds of customers attend INTERDATA's year-round training school. Additional training is provided on-site where requested. Courses pertinent to the Model 4 include: Software and Hardware instruction, FIRMWARE instruction, and a special course in maintenance.

Field Service Qualified factory trained personnel are at your disposal 24 hours a day should you experience difficulty with your Model 4, and they are as close as your nearest INTERDATA sales office.

Application Support For the many customers who require special support, INTERDATA offers a senior team of hardware, software, and FIRMWARE specialists whose background includes data acquisition systems, testing systems, process control systems, and data com-

munications. INTERDATA's sales engineers have long experience with small computer applications. They can give you valuable local assistance in planning and dimensioning your application.

Quality Control Quality Control at INTERDATA begins with detailed mechanical and electrical inspection of all components utilized in manufacturing a Model 4. Each stage

of assembly is carefully monitored through the employment of automatic and semi-automatic test equipment. Logic boards, for example, are checked with our own computers. In addition, ALL computers are given extensive environmental chamber evaluation prior to shipment. This total approach to Quality Control insures quick, trouble-free installation and a high degree of reliability.



Model 4

Basic Specifications

Data Word Length — 8, 16, 32 bits
(parity option)

Memory Cycle Time —
1.0 microsecond — Core Memory
400 nanosecond — Read-only-memory

Word Size — 16 bits

General Registers — 16 hardware
registers (16 bits each)

Hardware Index Registers — 15 general
registers may be used for indexing

Basic Memory — 4K bytes, expandable
to 65K bytes

Directly Addressable Memory — 65K bytes

Machine Code — Two's Complement

Instruction Repertoire — over 75 standard
instructions

16 bit—Load Halfword—2.8 microseconds

16 bit—Add Halfword—3.2 microseconds

16 bit—Multiply—3.8 microseconds
(optional)

Input/Output

Program Transfer — 25KBS

Block Transfer — 150 KBS (with high
speed option 4-101)
500 KBS (with selector
channel 7-201)

Interrupts — 2-256 levels
8 levels with arm/disarm
and mask (optional)

Display Panel

Control Switches — Power initialize
execute

Mode Control — Run, halt, single op,
variable speed, address input, memory
location, memory data

Speed Control — Variable, 1 cycle/sec
to 100 cycle/sec

Display — Two registers simultaneously
selectable

Switches — Sixteen data/sense

Mechanical

Size — 10 $\frac{1}{2}$ " x 19" x 4" (rack
mountable)

Power — 325 watts, 115 VAC \pm 10%,
47-63 hertz

Weight — 56 lbs.

Temperature:

Operating — 0° to 50°C

Storage — 55° to 85°C

Humidity — 0 to 90% relative

Reliability

MTBF — 6,000 hrs. (Mainframe and
4KB Memory)

Sales Offices

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