Memo 11

April 21, 1959

MEMO TO:

SUBJECT: STRETCH Performance

The enclosed File Memo is being sent to you with the hope that it may be useful in your talks with customers who are interested in smaller systems.

Please emphasize that the curves are approximate, based on typical problems only, etc., -- also it should be treated with the same confidence as the other STRETCH material you have received.

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April 21, 1959

PROJECT 7000

FILE MEMO

SUBJECT: The Dependence of STRETCH Internal Computing Speed on Various Configuration Parameters

## I. Introduction

There have recently been a number of requests for more information concerning the performance of STRETGH. Most of the requests have been for performance figures for STRETCH systems with other than 6 memory units and for an estimate of the effect on computing speed of Input-Output devices running at the same time.

The graphs presented here are based on Timing Simulator runs made on the IBM 704. Some of the points are from runs made especially for this report, others are based on various studies made last year.

It should be emphasized that the results presented in these graphs are smoothed and must be considered as approximate representations of how STRETCH will behave on typical examples. The actual percentages can vary considerably depending on the particular problem configuration being done.

## II. Speed vs. Number of Look-Ahead Levels

The Look-ahead serves as an internal buffer during the preparation and execution of instructions. Its main job is to allow STRETCH to use the overlapping asynchronous organization built into the computer design. It is a key factor in permitting a match of the high speed arithmetic circuits to the relatively slow memory units by multiplexing. It also has the important feature of serving as a "virtual memory" to avoid refetching repeated quantities from the main memory.

Graph I shows how the speed of STRETCH varies for one typical problem assuming different numbers of look-ahead levels in the design. "No levels" implies that the arithmetic unit is tied directly to the instruction preparation unit.

## III. Speed vs. Number of Memory Units

Graph II shows how internal computer performance varies with the total number of memory units for a particular problem. The entire calculation is assumed to be contained in memory for all cases.

The speed differential between having and not having instructions separated from data arises from delays in instruction fetches caused by the memory units being busy with data. The size of this effect varies from problem to problem, being less pronounced for problems which are arithmetic limited and more for logical problems.

Since memory units are attachable only in pairs after the first and are interlaced only in powers of two, some of the points on the graph do not represent physically attainable combinations, e.g., 5 memories all interlaced. The simulation program has no such restrictions.

## IV. The Effect on Internal Computing Speed of Simultaneous I/O Activity

Using the control word philosophy it is possible to have a number of input-output units operating at the same time the Central Processing Unit is running. The Basic Exchange can reach a peak rate of 1 word every 10 microseconds. The high speed disk normally operates at 1 word every 4 microseconds. Since the mechanical devices take priority over the CPU in addressing memory, the computation slows down because of memory-busy conflicts.

Graph III shows an example of how internal computing speed is slowed as the I/O word rates are varied continuously, at the theoretical "choke off" the I/O devices take all the memory cycles available and stop the calculation. Notice that this condition can never arise for any I/O rates presently attainable.

## V. The Effect of the High Speed Disk

Because there are fewer memory cycles available when there are fewer memory units, the disk unit will cause a larger percentage slow-down for a smaller system. Graphs IV and V show this effect for two typical problems--one which is normally arithmetic limited and one which is instruction-fetch limited. The former is less sensitive to such interference mainly because look-ahead has more of an averaging effect on its data memory references.

The following table shows the reduction in internal computing speed caused by the disk, using the speed without I/O as 100% for each configuration.

The effect of the High Speed Disk on STRETCH Speed:
(Approximate reduction in speed of internal computation for systems with different numbers of memory units caused by disk running at the same time.)

| Number of Memories | For Monte Carlo Problem | For Reactor Problem |
|---|---|---|
| 6 | - 5% | - 2% |
| 4 | -15% | - 4% |
| 2 | -24% | -22% |
| 1 | -55% | -55% |

This indicates that the user of a small system is penalized twice: once by a reduction of the top speed of his system and again by a larger I/O penalty when it is run concurrently with the computation.

In all fairness, however, the above reductions in performance with I/O running are still far preferable than stopping CPU activity completely as the 704 does, particularly when one contrasts the information flow rates involved.

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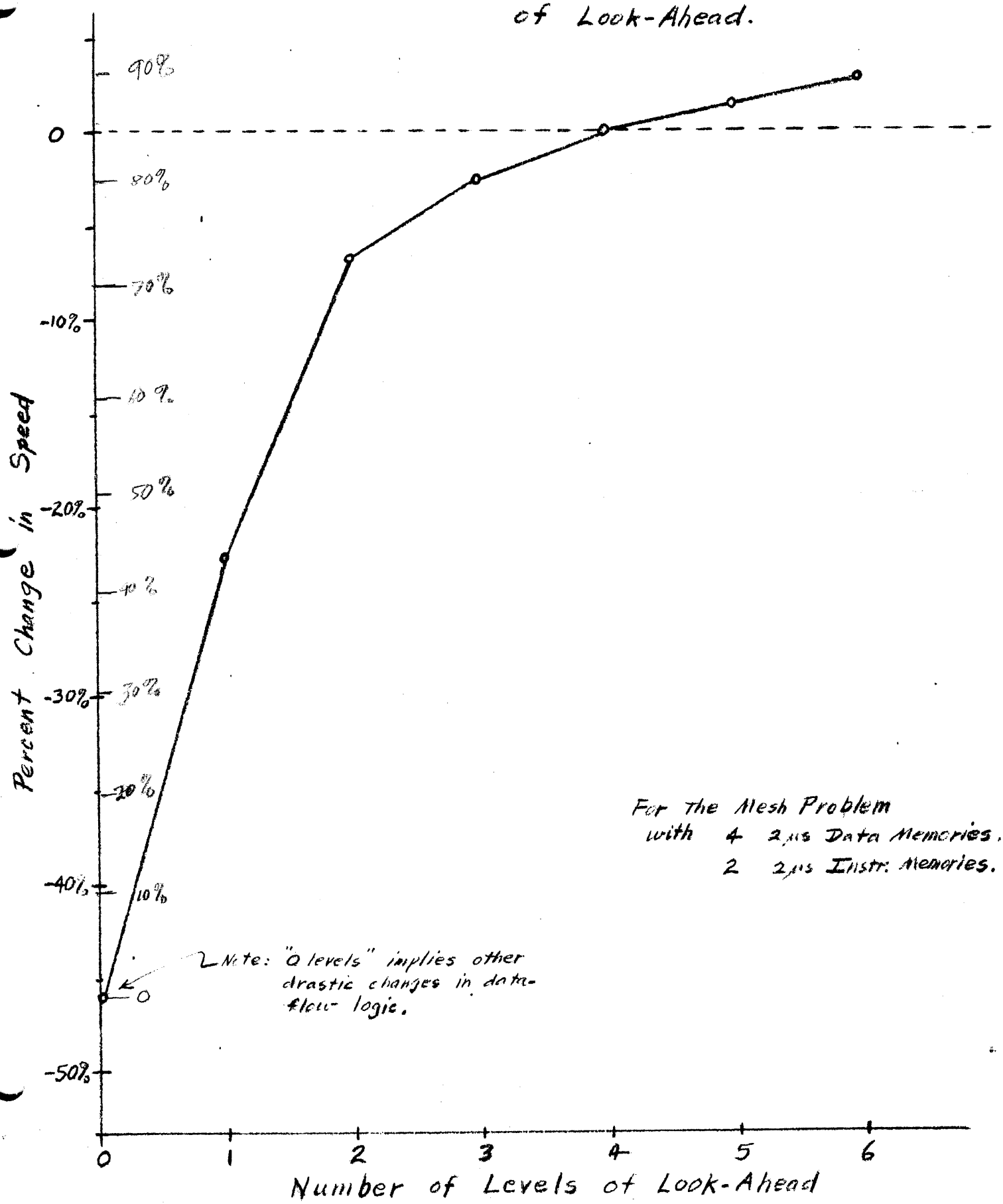
Enclosures: 5 Graphs

Graph I

(Mesh Prob.)

# STRETCH: Speed of Internal Computation vs. Number of Levels of Look-Ahead.




For the Mesh Problem
with 4 2 μs Data Memories.
2 2 μs Instr. Memories.

Note: "0 levels" implies other drastic changes in data-flow logic.

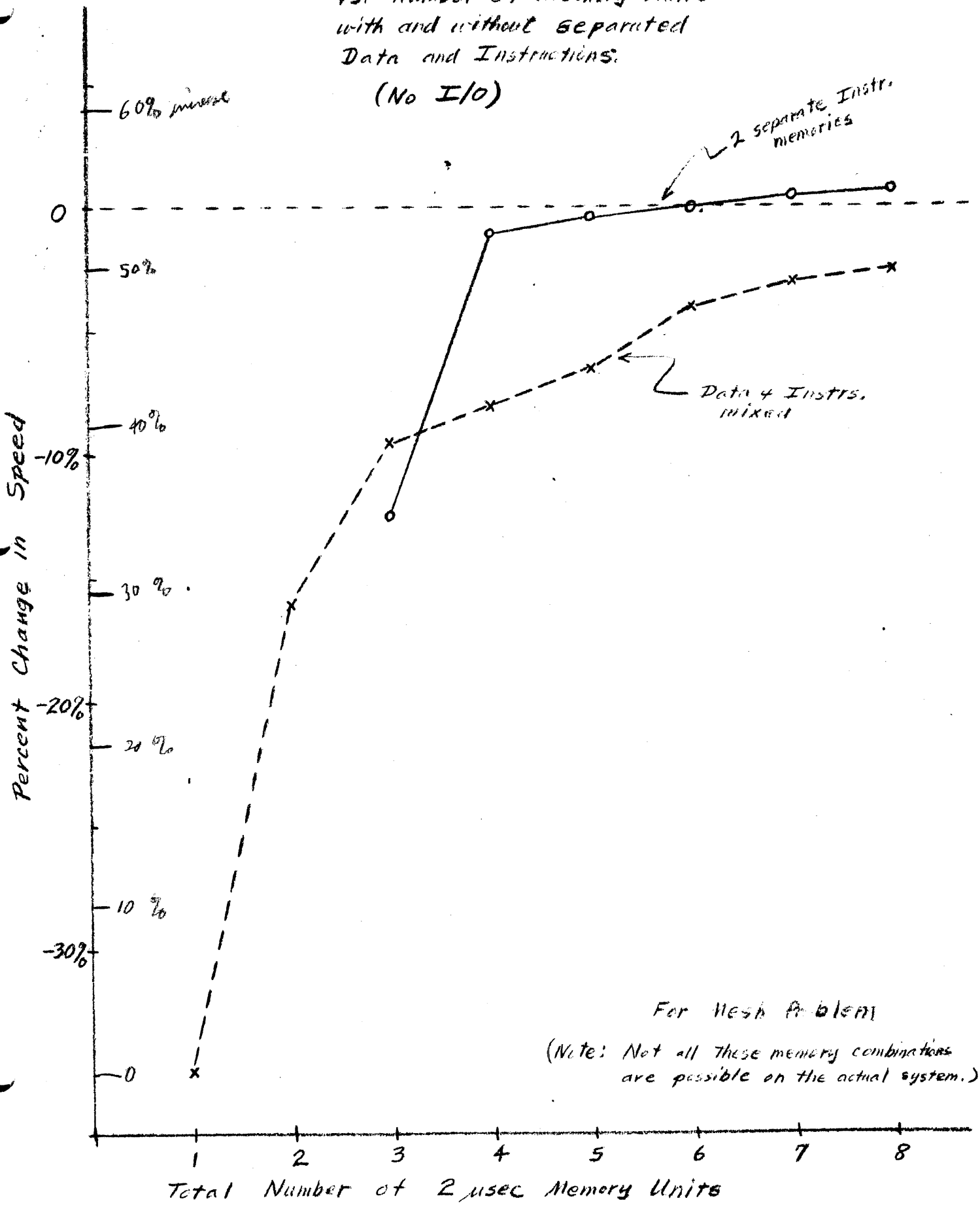
HGK Apr 3.'59

# Graph II

(Mesh Prob.)

STRETCH: Speed of Internal Computation vs. Number of Memory Units with and without Separated Data and Instructions.

(No I/O)



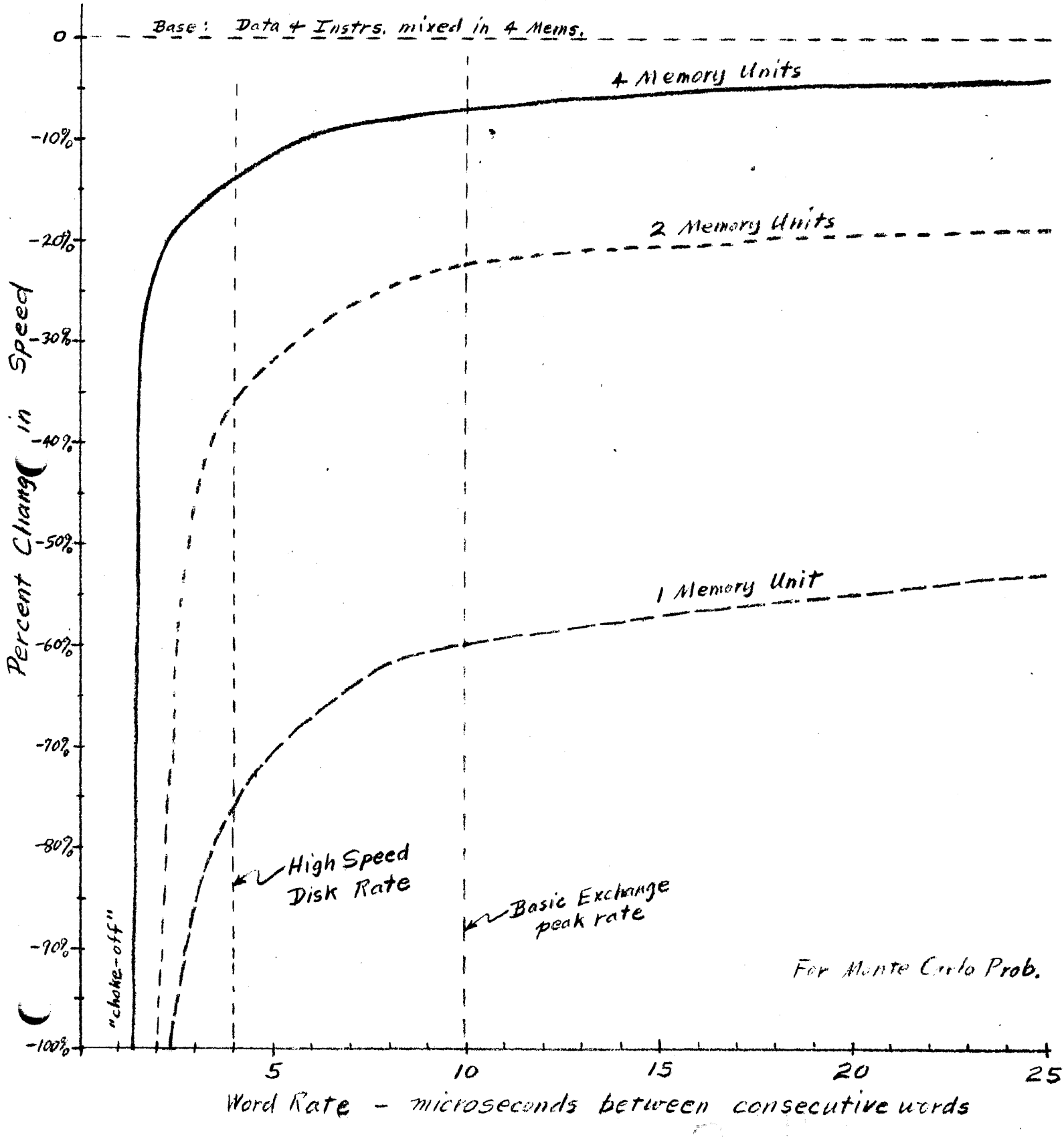

For Mesh Problem

(Note: Not all these memory combinations are possible on the actual system.)

Graph III

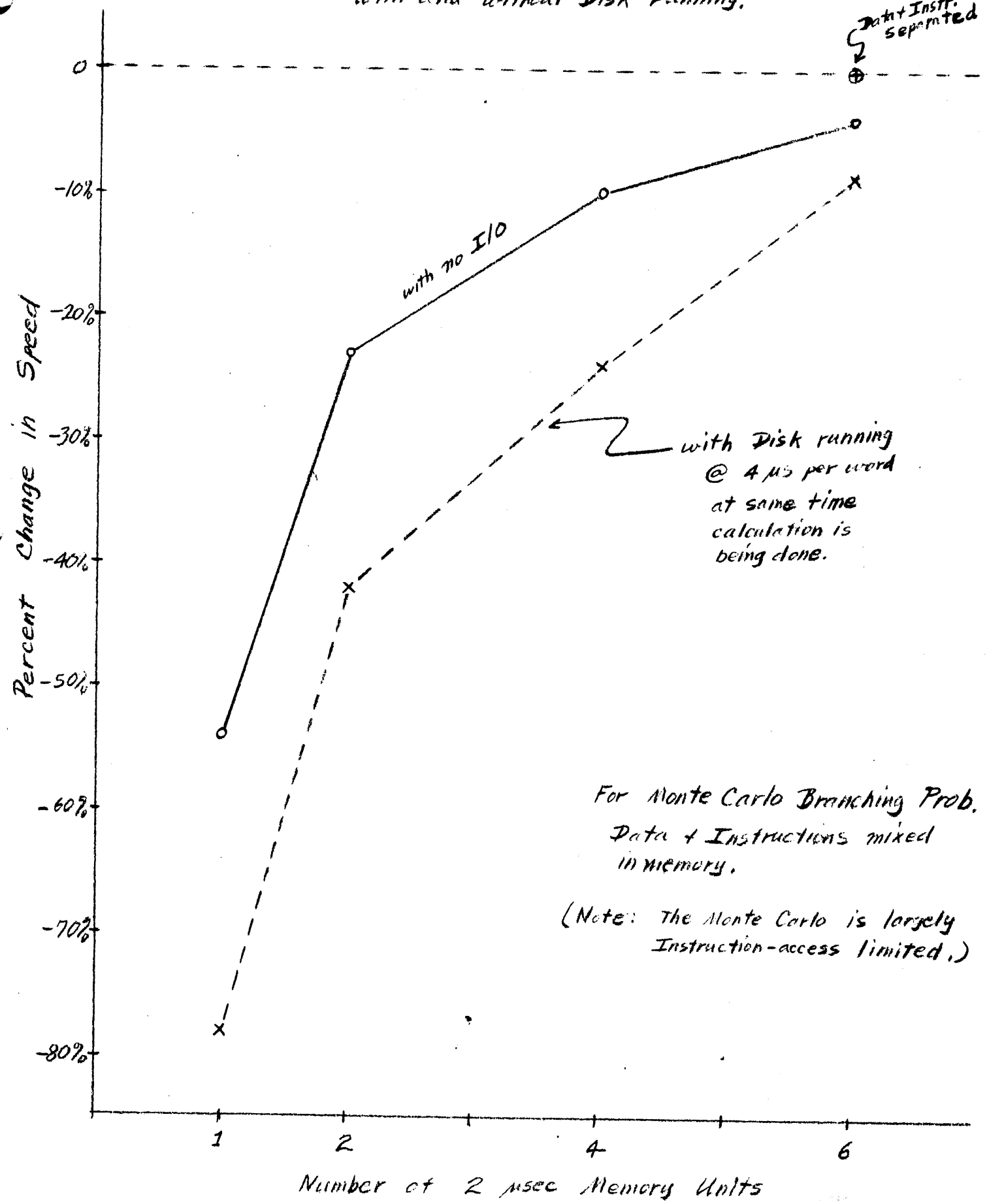
STRETCH: Internal Computing Speed. (Monte Carlo)

Percentage Reduction in Speed caused by Input-Output devices referencing memory at different rates while the calculation is proceeding.



Graph IV

STRETCH: Speed of Internal Computation vs. Number of Memory Units with and without Disk running. (Monte Carlo)



Graph V

STRETCH: Speed of Internal Computation (Reactor Prob.)
vs. Number of Memory Units
with and without Disk running