May 20, 1958

MEMO TO: Mr. S. W. Dunwell

SUBJECT: Memory Cycle Times and Their Effect on SIGMA Performance

There is an area which has not received much attention of late in our discussions of performance but which can have as serious an effect on the SIGMA system as the arithmetic speeds. I am referring to the memory times.

In John Cocke's and my Memo, "A list of some 5% Effects" dated April 18, 1958, we pointed out that SIGMA performance decreases by 5% when the read-out time for the 2.0 usec memory increases from the nominal 0.8 us to 1.2 us. This was true for a relatively "sluggish" system. If contract AU speeds are used the percentage change is even greater (for example: see graph 2 of my memo on "Branching on Arithmetic Results" dated May 19, 1958).

The effect of the total memory cycle time (keeping read-out time fixed) is harder to assess. It has relatively little effect on problems which are heavy on arithmetic, but a serious effect on problems of the logical type.

In talking to Mr. Wheelock, I find that the present theoretical estimates (based on experimental evidence) for the 2 usec memory are: Read-out Time no earlier than 1.05 usec, Total cycle Time 2.25 ± 0.25 usec.

Since the memory buses are presently timed so that the memory can read out only in intervals of 0.3 usec, this could mean that the true memory read-out time is 1.2 usec instead of 1.05. (assuming they are 0 together.)

It is important that the 2 usec memory and the bus system as well as the half usec and the index memories do not compromise the advances being made in the AU and IAU area.

I would appreciate your comments or suggestions.

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