Super-Stretch Memos

T. C. Chen's Memos on 7030 * (STAR) (or K-9 "Dog")

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Memorandum to: Dr. S. G. Campbell

Subject: Index Word Format and Index Arithmetic

The purpose of this memo is to point out some improvements possible by removing the incompatibility between index value field format and instruction address field in the 7030.

The 7030 index value field has a sign bit besides the 24 numeric bits. The reason for this sign bit is to clearly distinguish between augmentation and decrementation in the creation of effective addresses, and to provide programming flexibility not heretofore available.

The sign bit, however, creates a basic incompatibility between the index value field and the (unsigned) numeric address field in instructions. The hardware treatment seems unnatural to the uninitiated programmer. More important, this incompatibility entails hardware cost, some complications, and injection of several instructions not needed otherwise. The gain in clarity and flexibility seems to be insufficient to justify the difficulties.

During the creation of an effective address, the numeric address field is made to behave as if it has a positive sign in the algebraic addition. The (24 bit + sign) effective address, however, is not the execution address; in particular the sign bit must be ignored. The new 7030 programmer is often bewildered by the temporary interjection and subsequent removal of the sign. Further, all "load value" type instructions (LV, LVE) put 25 (24 + sign) bits in the index value field, and it is dangerous practice to use an instruction address field to furnish information to index value fields.

In terms of hardware, the presence of a sign bit means not only an extra bit to handle, but requires new instructions to ensure the proper management of index sign. Examples are:

V - I, V - IC, V - ICR
LVNI, KVNI, C - I
plus options (V - I), (V - IC), and (V - ICR) in progressive indexing.

These operations can be deleted from the 7030 repertoire without any loss of performance if the sign incompatibility is removed.

A further complication is that the use of repeated signed arithmetic should be accompanied by some overflow allowance and/or detection devices. In the absence of these, multiple indexing operations (such as LVS) will lack commutability. For instance, given positive quantities A, B and C, if $A > C$, $B > C$ one may still have $(A+B) - C < 0$ due to overflow. $A + (B - C)$ is of course still positive.

The programming flexibility due to the index field sign is subtle and hard to exploit. For example, since the execution address ignores the sign bit, it is possible to use a large negative value field to index a small numeric address, and the latter behaves ultimately as a negative address. This usually merely means one more programming alternative with little significant advantage over others.

The value field-address field incompatibility can be resolved in either of two ways:

1) Provide a sign in the address field. This does not solve the overflow difficulty. The assignment of special register addresses is likely to be delicate, as the region 0 through 31 is now in the middle of the memory address range, and the old assignment tends to cut the memory space in half.

2) Remove the sign bit from the index value field, and rely on 2's complement arithmetic. This scheme avoids most of the pitfalls, simplifies programming education, instruction decoding and hardware.

It is to be noted that the STRAP assembler translates negative addresses automatically into 2's complements, and the value field sign so far has not obviated the need for complement addresses.

Incidentally, if the convention is adopted that a zero refill field means "do not refill", the following operations can again be removed, the "refilling" counterparts alone will be sufficient.

V+ IC, V+ C, CB
and the option (V + IC) in progressive indexing.

Altogether there will be nine operation deletions, and four progressive indexing options. These changes hopefully will allow the installment of the badly needed operations such as V -, V - CR, SHVA (shift value), and features like indexability of immediate index instructions.

The idea of the last paragraph was due to G. R. Hira and C. T. Apple. Most of the material in this memo resulted from a discussion with C. T. Apple, and has been checked for feasibility with G. R. Hira, C. L. Gerberich, and J. L. Garrity, as well as D. H. Gibson and R. L. Rockefeller of Kingston during the week of June 26, 1961.

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