MEETING OR CONTACT REPORT

	Date of Report: May 27, 1958
Organization & Location:	
BuShips	Date: May 21, 1958
BuShips Bldg., Fort Mead, Maryland	Reported By: H. G. Kelsky
Project:	
	Department: 749
STRETCH - HARVEST	Follow-up Date: June 2 1958

PERSONNEL PARTICIPATING: (Place asterisk next to those on distribution list. Other distribution show at end of report)

BuShips		IBM
*Representatives		Representatives
T. McCool		H. G. Kolsky
J. Willard		J. Cocke *
D. Oppert		N. Blazensky*
J. O'Hara		
S. Snyder),		
S. Snyder (were prese	nt part-time	only)

The meeting was called to discuss the SIGMA timing simulator and its possible use in determining some of the performance specifications for the HARVEST computer.

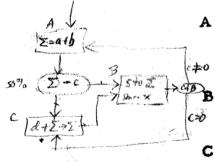
The first part of the meeting consisted of a description by Kolsky and Cocke of the SIGMA Timing Simulator and a qualitative discussion of the results which have been obtained by it. The shapes of various performance curves such as speed vs number of memory boxes, etc., were sketched, although no exact performance figures were quoted.

The Simulator consists of approximately 2200 words of 704 code and requires a 4096 word memory, along with two tapes and one logical drum. The program can be easily modified to use all core memory instead of cores and drum. The Simulator draws "Timing Charts" which show the activity of the various components of the computer system vs time. The timing considerations and interlocks existing in the actual circuits are simulated in the code. Samples of code which run about 1000 usec. on the actual computer can be simulated in about five minutes on the 704 if only summary information is printed.

The second part of the meeting was devoted to discussing the types
of problems which should be done on the Simulator to provide the
desired figures.

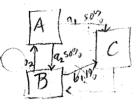
The list of problems decided upon, in the order of priority, are:

- (1) A series of ADD's. A series of MPY's. A series of DIV's.
- (2) A series of LOAD, ADD, STORE's
- (3) A series of LOAD, STORE's (Bit transmit)
- (4) A series of LOAD, ADD TO MEM's.
- (5) The following sample program:



LOAD
ADD
COMPARE
IND BRANCHTO C
STORE
INCR INDEX
COUNT AND BRANCH TO A
ADD
BRANCH TO B

(6) A Matrix Multiply Inner Loop.



B

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The above are all for VFL data. Several should be done for field lengths of 8, 16, 32, 48, 64 bits to get the performance dependence on field length. Numbers (1) and (2) should be done over with:

- (a) Data in Main Memory, instructions in Fast Memory.
- (b) Data in Fast Memory., instructions in Main Memory.
- (c) Data and instructions intermixed in Main Memory.
- (d) Data and instructions intermixed in Fast Memory.
- (c) Case (c) varying the number of Main Memories from 1 to 8.

To get an estimate of the effect on Computer Performance of operating high speed tapes that the high speed exchange plus a variable number of units on a low speed exchange, some of the above problems will be run with the following combinations:

- (a) High Speed Exchange reading and writing. (assume approximately 7.1 usec per pair of words read and written)
- (b) Low Speed Exchange reading and writing with various average word rates assumed.
- (c) A combination of (a) and (b).

Some of the above cases will be coded and timed in 704 language to give a direct comparison of the HARVEST computer speeds vs 704 speed.

- 3. It was agreed that after the above programs had been studied that there would be considerable interest in evaluating the computer performance for the following:
 - (a) Coded versions of the HARVEST Streaming Mode operations, such as Stream Merge.
 - (b) A Coded version of the Stream Multiple Table Look-up operation.

4. The necessary changes in the Simulator to handle the two exchange meck-ups etc., will require about a week. Work will then start on the actual programs listed in paragraph 2.

A progress report will be made to BuShips on June 2, 1958.

Hawood & Kaloky

Product Planning Representative

Project 7000

HGK/jev

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