MEETING OR CONTACT REPORT

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Organization & Location: Product Development - IBM Poughkeepsie	Date: March 21, 1958 Reported By: H. G. Kolsky
Project: STRETCH SIGMA Performance	Department: 749 Follow-up Date:

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1. Purpose of Meeting: To discuss the present status of SIGMA performance and to inquire into possible methods of improving it.

2. Present Status:

   a. Simulation studies (Reference: Project 7000 File Memos, dated February 6, 1958, and March 12, 1958 by Kolsky and Cocke) indicate that SIGMA performance on the internal computing sections of typical problems to be in the range 40 to 80 times 704 speed. The lower speeds occur for problems containing a lot of branching and index modification. The higher speeds for problems heavy on floating point arithmetic. The speeds discussed early in the STRETCH program were 100 to 150 times 704 speed.

   b. The SIGMA arithmetic unit speed is a separate problem. It is presently under study and a data flow model will be built to establish the actual speeds with which such circuits operate. Every effort will be made to use standard pluggable units and frames, but we will depart from them if necessary to make the speeds.

c. The Indexing Arithmetic unit is in final stages of design. The interconnections with Look Ahead have been largely defined. Regular instruction preparation is limited to a 0.9 usec rate. Any reduction below 0.9 usec seems to be expensive. The I-Box is tied to the basic 0.8 usec cycle core storage with 0.4 usec read-out time. Several operations occur in parallel with this cycle. The actual index addition takes 0.6 usec, transfers between registers require 0.3 usec.

The I-Box design would have to be reorganized to operate at a faster index core rate. 0.3 usec is the minimum read-out time possible since this is the inter-register transfer time.

3. Discussion of Status: The question was raised as to what has caused the apparant reduction in speeds during the past year. Some of the reasons are:

(1) The early speed estimates did not assume the realistic complexity in design which the present machine studies do.

(2) The fundamental circuit speeds are slower by a factor of 2 to 4.

(3) The memories are all slower: The Main Data memory cycle is being quoted at 2.2 usec instead of 2.0 usec, with a read-out at 1.2 usec instead of 0.8 usec. The Fast Instruction Memory has a cycle time of 0.6 to 0.75 usec instead of 0.5 usec. The Index Memory has a cycle time of 0.8 usec (if cores are used) instead of 0.2 usec.

(4) The bus times and checking times which add linearly to most instruction and data transmission times are running 0.8 to 1.0 usec instead of 0.2 usec.

4. Possible Methods of improving Performance:

(a) The fundamental circuit speeds should be the best we can do. Possible improvements in logical layout will be examined.

(b) The core memory cycle times should also be the best we can do. Some increase in speed may be possible but with greater heating problems.

(c) Index Memory: Cores or transistor Registers?
The Indexing Arithmetic Unit sees only the 0.4 usec read-out time on ordinary indexed instruction modification. On Increment or Count type orders the 0.8 usec total cycle time is more important because there is both a fetch and a store index word. The effect of using cores instead of transistor registers should be examined for economy reasons, but the resulting decrease in performance must be unimportant. Present Simulation results show about a 10% effect on speed.

(d) A design of the SIGMA I-Box separate from that of the BASIC computer might make a considerable improvement in the over-all performance. This should be examined.

(e) Multiple accumulators. The possibility of using multiple accumulators in the arithmetic unit, in the same manner as LARC, was raised as an alternative to transistor index registers. The complications in instruction set and circuit controls seem to preclude this possiblity unless we go to full word instructions.

(f) A separate small core array tied directly to the look-ahead for intermediate data storage was proposed to reduce the interference of data stores from Look-Ahead with indexed instruction preparation. One main difficulty here is the loss of homogeniety of memory which we presently have. One simulator run indicates this improves performance about 5%.

(g) A small separate instruction memory tied directly to the indexing Arithmetic Unit was also discussed. It also destroys memory homogeniety since it presumably could be loaded only by "transmit" instructions. Its effect should be simulated.

(h) A large read-only memory tied directly to the IAU was also mentioned as a possibility.

(i) A suggestion was made to improve the performance on indicator branches by assuming the branch is taken if "Branch on" is written. This requires a study of the indicators available to see if ≥ 0 and ≤ 0 indicators can be included in the list.

(j) The I-Box should test the Indicator branches having to do with index results and fetch the next correct instruction rather than guessing.

5. Conclusions: It does not seem desirable to make any drastic changes in the SIGMA design philosophy, such as going to full word instructions, etc., at this date.

We must be alert to avoid any situations in the design which might prevent the computer system from taking advantage of future gains in one or another component.

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