SIGMA COMPUTER MEMO #8

SUBJECT: Applications of Sequential Circuit Synthesis

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A sequential switching circuit is one with a memory. That is, at any bit-time the state of each output is a function not only of its present state of all the inputs, but also of inputs in the past. When several function generators are interconnected so that feedback loops exist, the composite switching circuit, called a sequential circuit, may exhibit memory.

The advantage of using the sequential synthesis approach over the trial and error method in deriving circuits with a memory is that the sequential circuit may be translated into exact formalized description. Next the description may be manipulated so that is is possible to recognize what interconnections of function generators will give a corresponding circuit. It is possible to derive where to put the feedback connections, and how many generators are necessary.

Using the synthesis method which is reviewed by D. A. Huffman, in Technical Report No. 274, Research Laboratory of Electronics, M. I. T., January 10, 1954, the following circuits have been derived:

A. Gated trigger with bipolar set
B. Binary Flip Flop
C. Gated two way exclusive OR trigger
D. Gated three way exclusive OR trigger (not shown here)
E. Escapement gate and trigger

Attached are the circuit requirements and logical block configurations.

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A. Gated Trigger with Bipolar Set

Figure 1 and 2

1. The data signal has to be present on the input of the trigger at the time the gate goes positive, and may not change until the gate signal is negative. If the data signal changes two logical stage delays later, the output will change.

2. To set new data into the trigger the gate signal shall be positive for a time period equal to or greater than the delay of two logical stages. The gated trigger with bipolar set is a two level hazard free circuit. (i.e. - not dependent on relative speeds of logical blocks)

B. Binary Flip-Flop

Figure 3 and 5

This is not a hazard free circuit. The circuit has a "static" hazard present during the change of X (data input), which introduces a complementary value on the output for a short interval. The hazard may be overcome by inserting a delay line on the output of logical block marked "K".

The circuit requirement is that the data signal be present on the input of the binary flip flop for a time period equal to or greater than the delay of two logical stages, which will set (reset) the binary flip flop.

Figure 4 and 6

The circuit performs the same functions as the one in figure 3 and 5, except that this is a hazard free circuit and no delay line is required. The circuit requirements are the same as in figures 3 and 5.

C. Gated Two Way Exclusive OR Trigger

Figure 7 and 8

This is a hazard free circuit. The circuit performs a two way exclusive or on inputs X_2 and X_3, gating and storing in two logical levels of delay. The circuit requirements are the same as in figures 1 and 2.

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E. Escapement Gate and Trigger

Figure 9 and 11

This is not a hazard free circuit.
Circuit requirements:

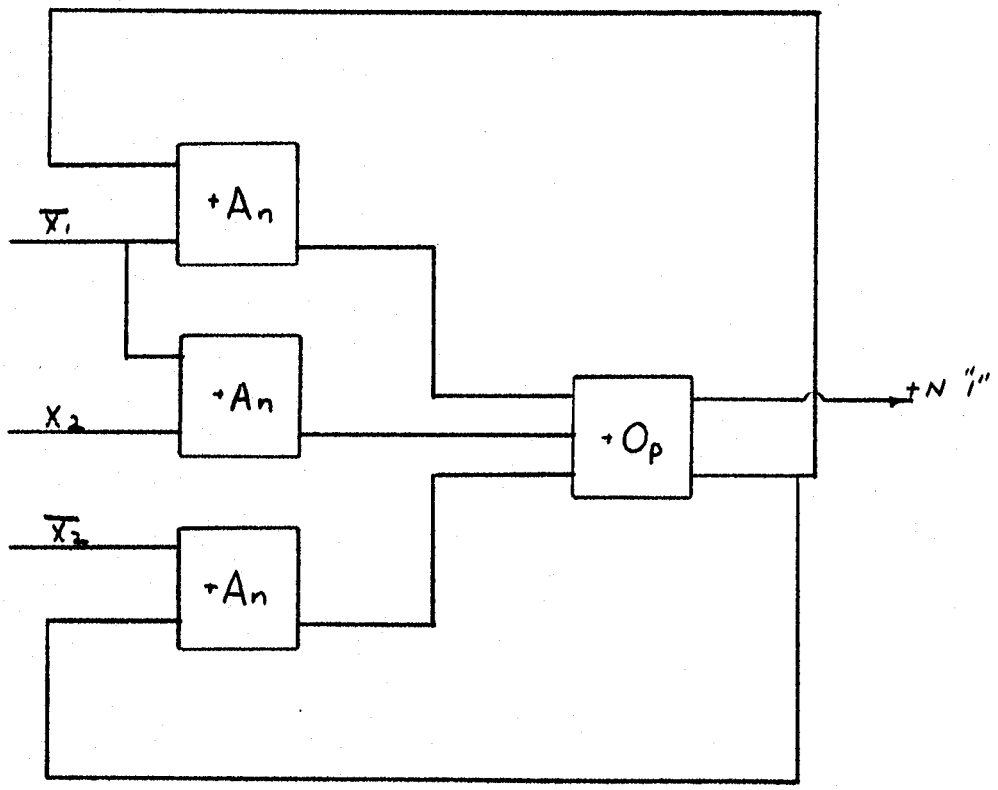
1. The data signal has to be present for two logical levels of delay before the gating signal is applied and one logical stage delay after the gate signal has been applied.

2. The gate signal shall be positive for the time period equal to or greater than the delay of two logical stages.

Figure 10 and 12

The advantage of this circuit over the circuit on figure 9 and 11 is that this is a hazard free circuit. The circuit requirements are the same as in figures 9 and 11. (see above)

FIG. 1 GATED TRIGGER WITH BIPOLAR SET



13 TRANSISTORS

2 LEVELS

X_1 = DATA SIGNAL

X_2 = GATE SIGNAL

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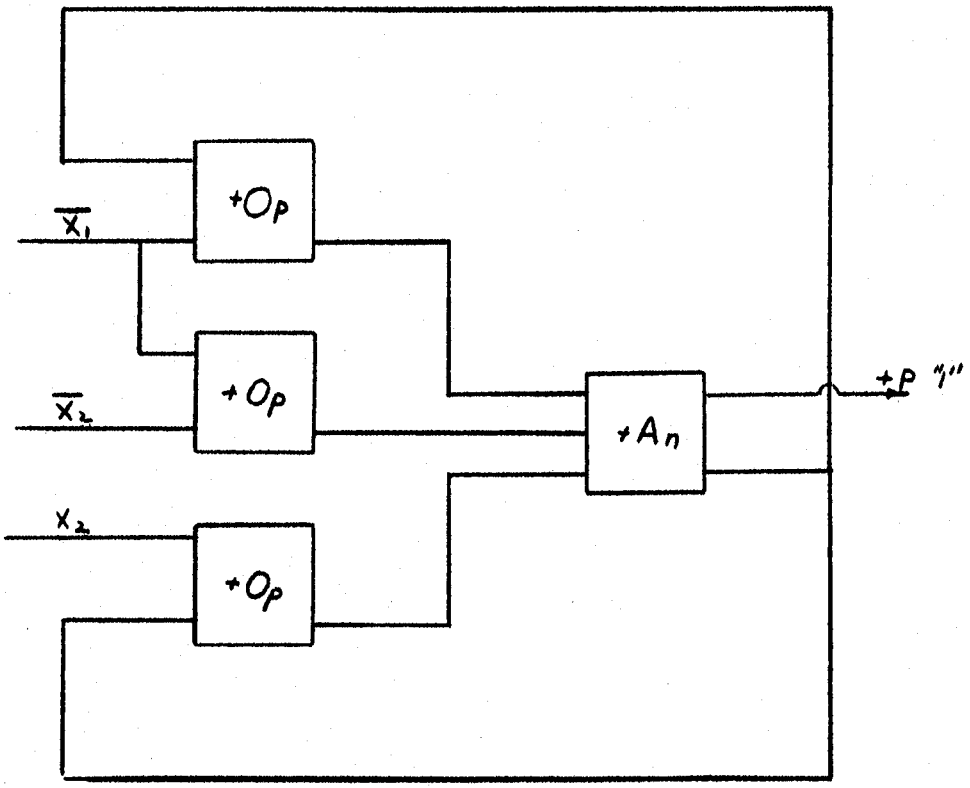
FIG. 2

GATED TRIGGER WITH BIPOLAR SET



13 TRANSISTORS

2 LEVELS

X_1 = DATA SIGNAL

X_2 = GATE SIGNAL

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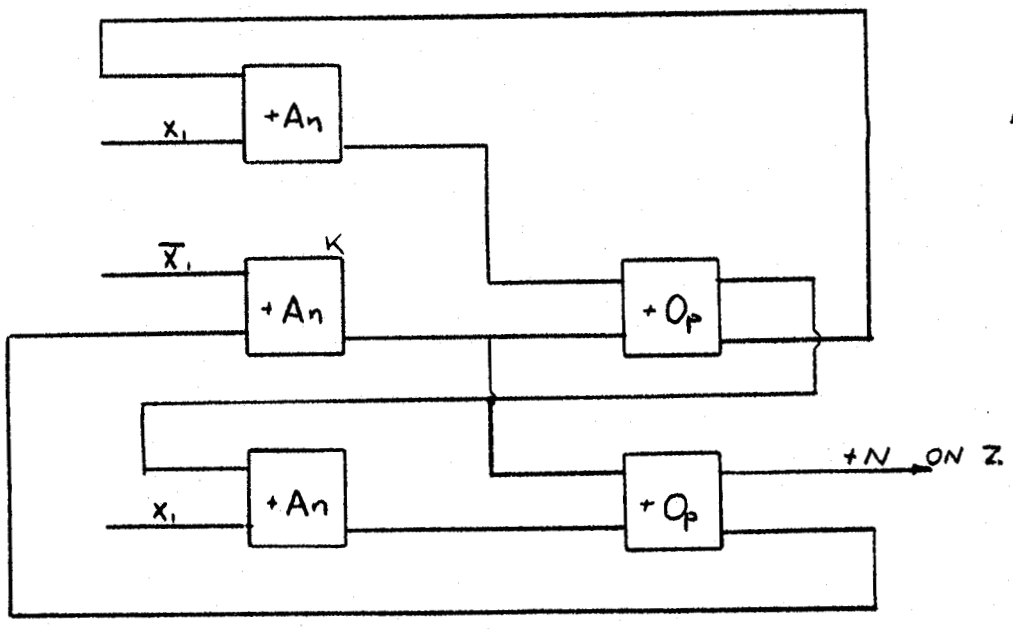
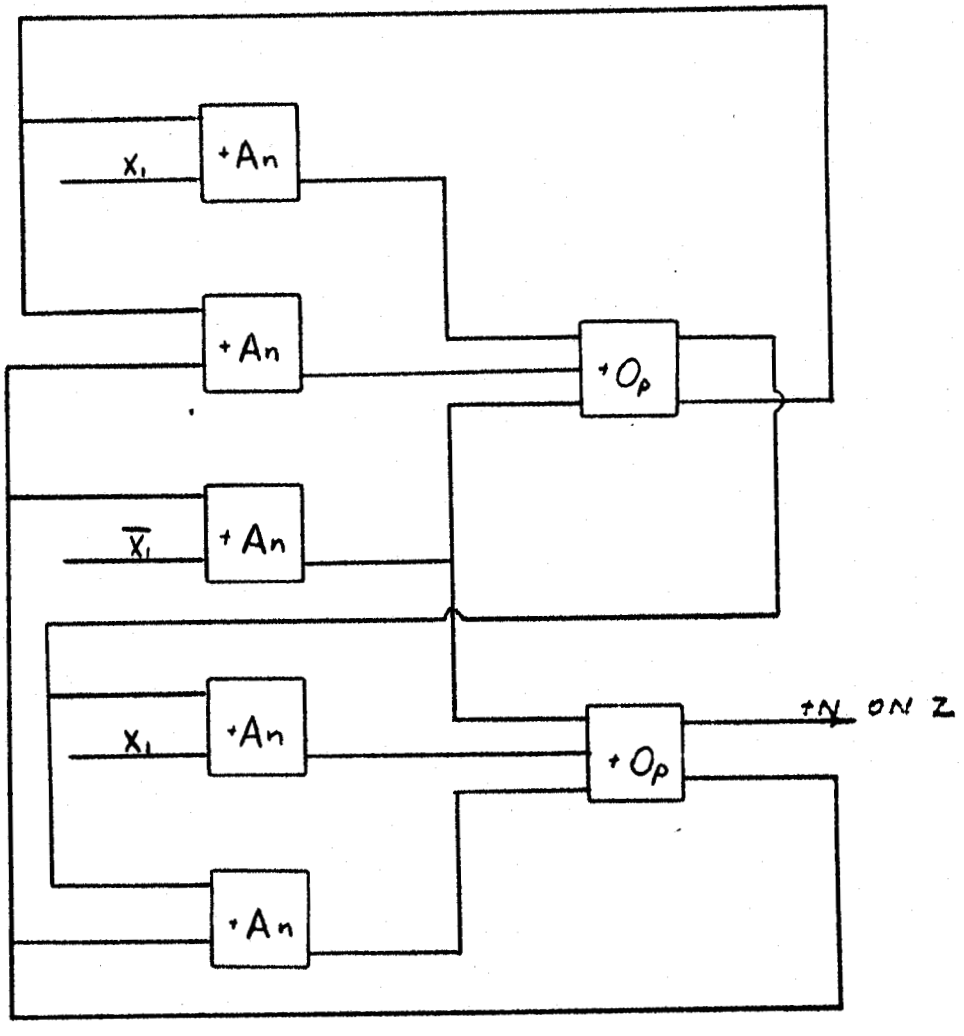
BINARY FLIP-FLOP

FIG. 3



15 TRANSISTORS
2 LEVELS
X_1 = DATA SIGNAL
Z = OUTPUT

FIG. 4



23 TRANSISTORS
2 LEVELS
X_1 = DATA SIGNAL
Z = OUTPUT

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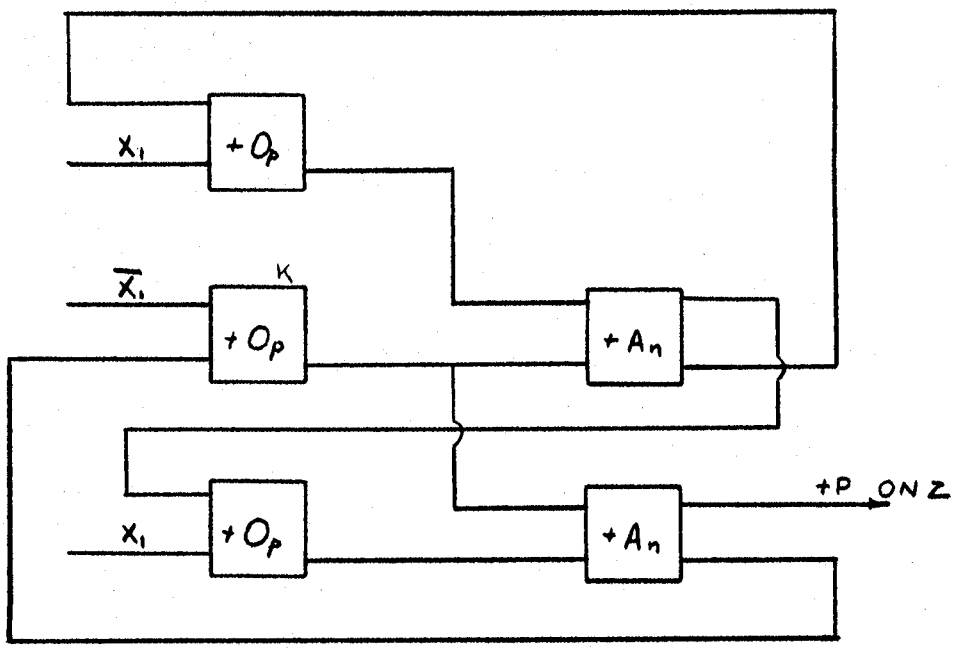
FIG. 5

BINARY FLIP-FLOP



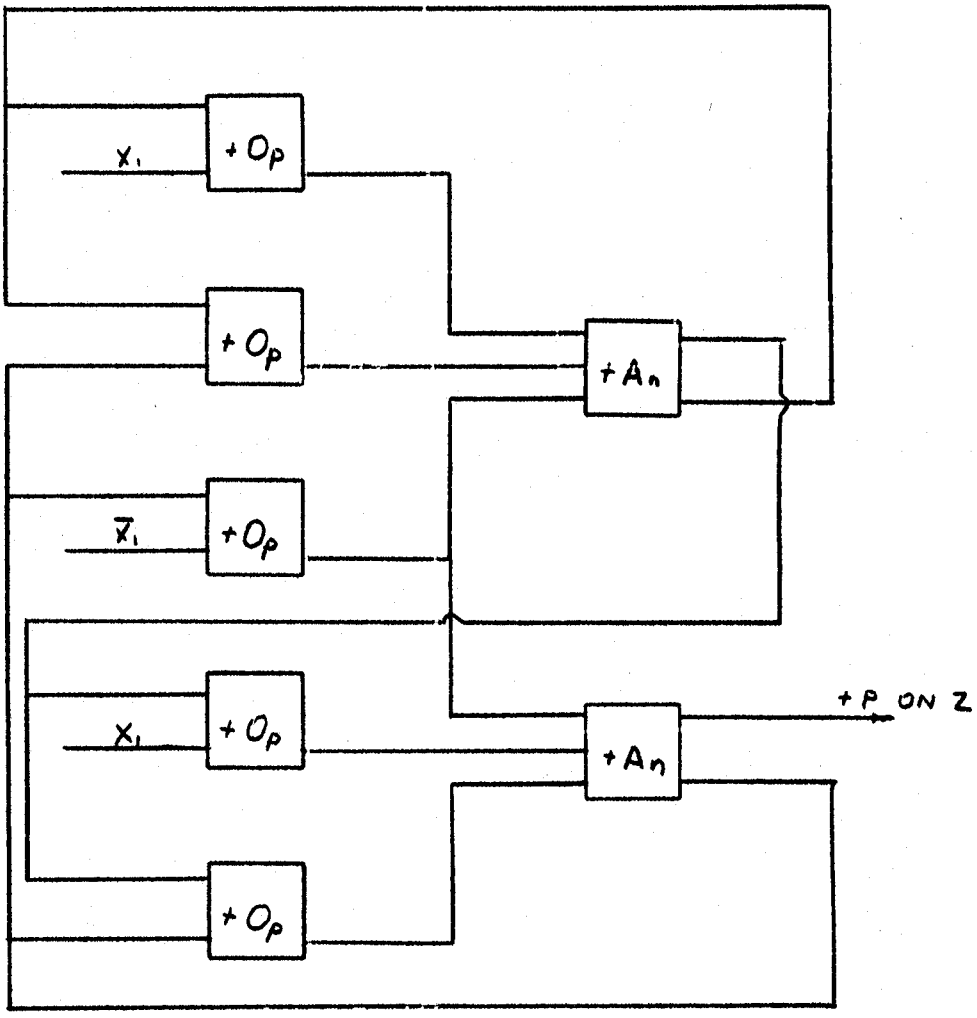
15 TRANSISTORS

2 LEVELS

X_1 = DATA SIGNAL

Z = OUTPUT

FIG. 6



23 TRANSISTORS

2 LEVELS

X_1 = DATA SIGNAL

Z = OUTPUT

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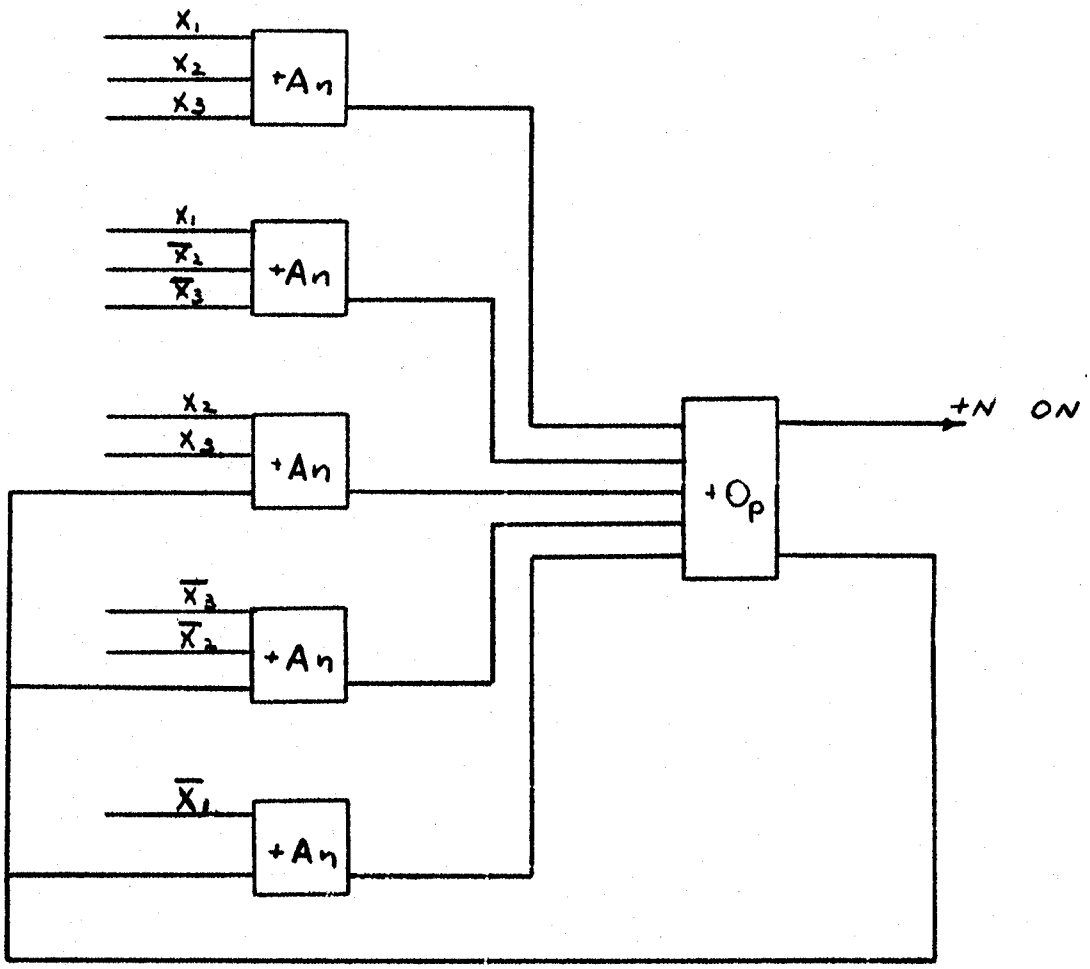
FIG. 1

GATED TWO-WAY EXCLUSIVE OR TRIGGER



25 TRANSISTORS

2 LEVELS

X_1 = GATE SIGNAL

X_2 & X_3 = DATA SIGNAL

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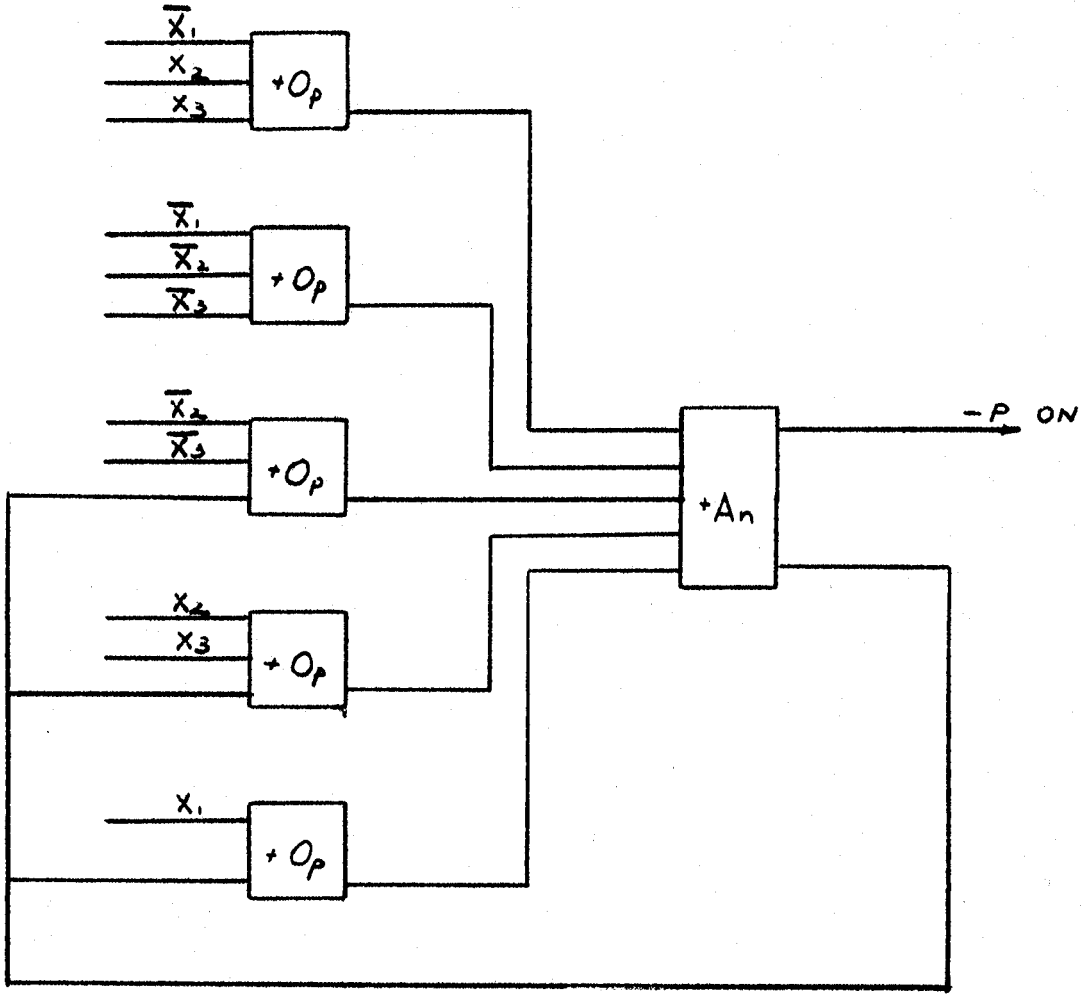
GATED TWO WAY
EXCLUSIVE OR TRIGGER

FIG. 8



25 TRANSISTORS

X_1 = GATE SIGNAL

X_2 & X_3 = DATA SIGNAL

2 LEVELS

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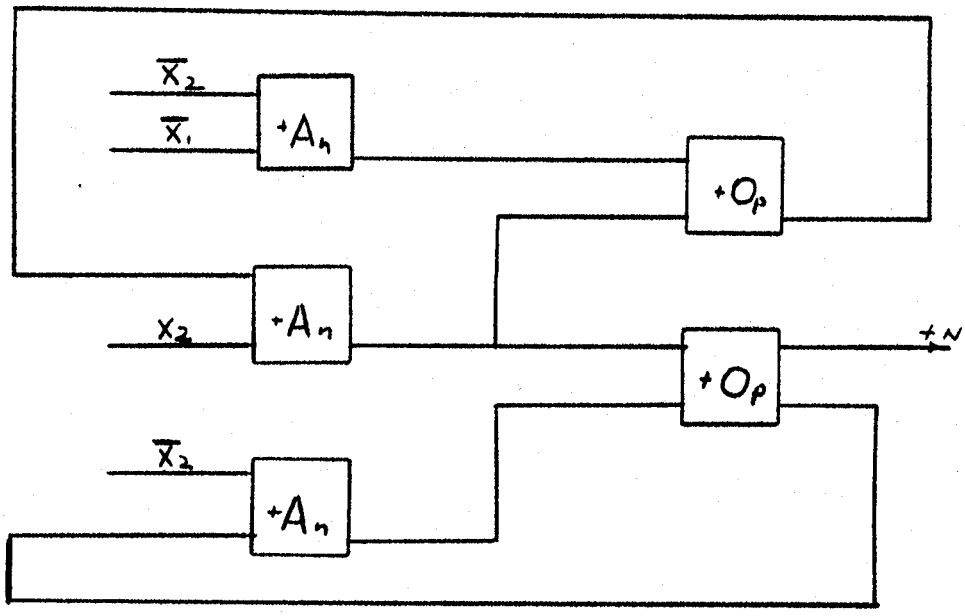
FIG. 9

ESCAPEMENT GATE AND TRIGGER



15 TRANSISTORS

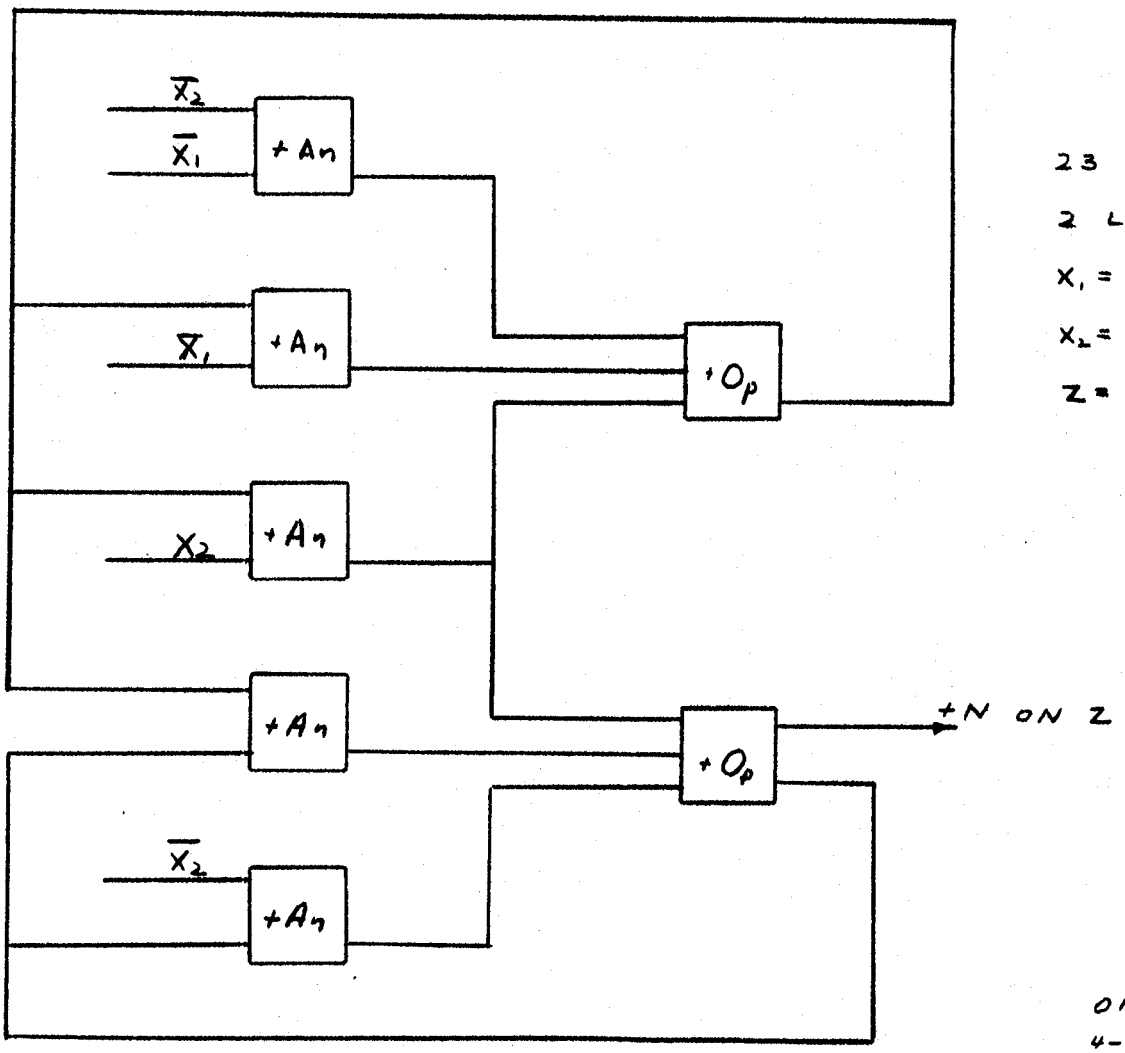
2 LEVELS

X_1 = DATA SIGNAL

X_2 = GATE SIGNAL

Z = OUTPUT

FIG. 10



23 TRANSISTORS

2 LEVELS

X_1 = DATA SIGNAL

X_2 = GATE SIGNAL

Z = OUTPUT

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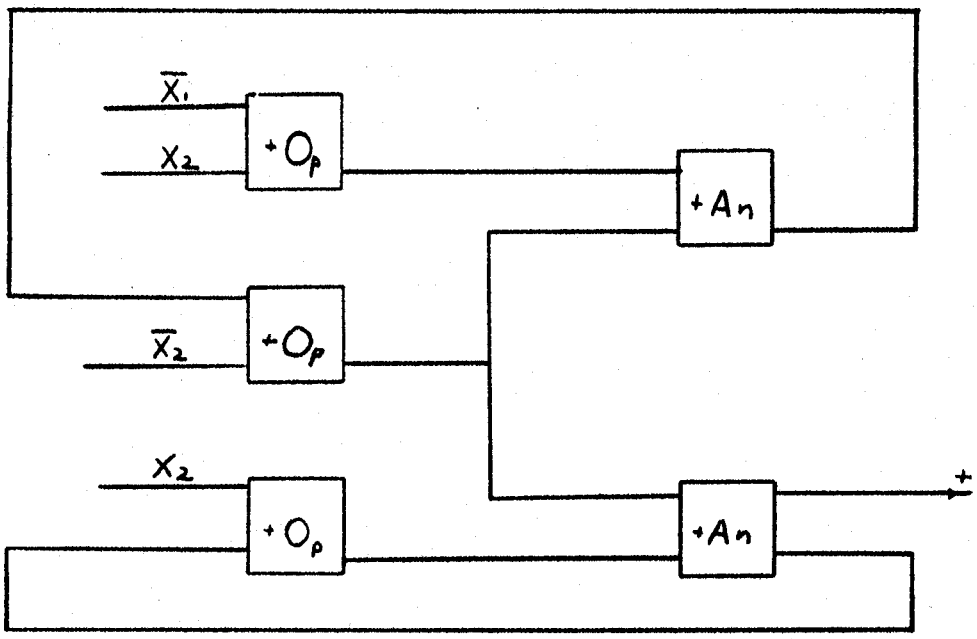
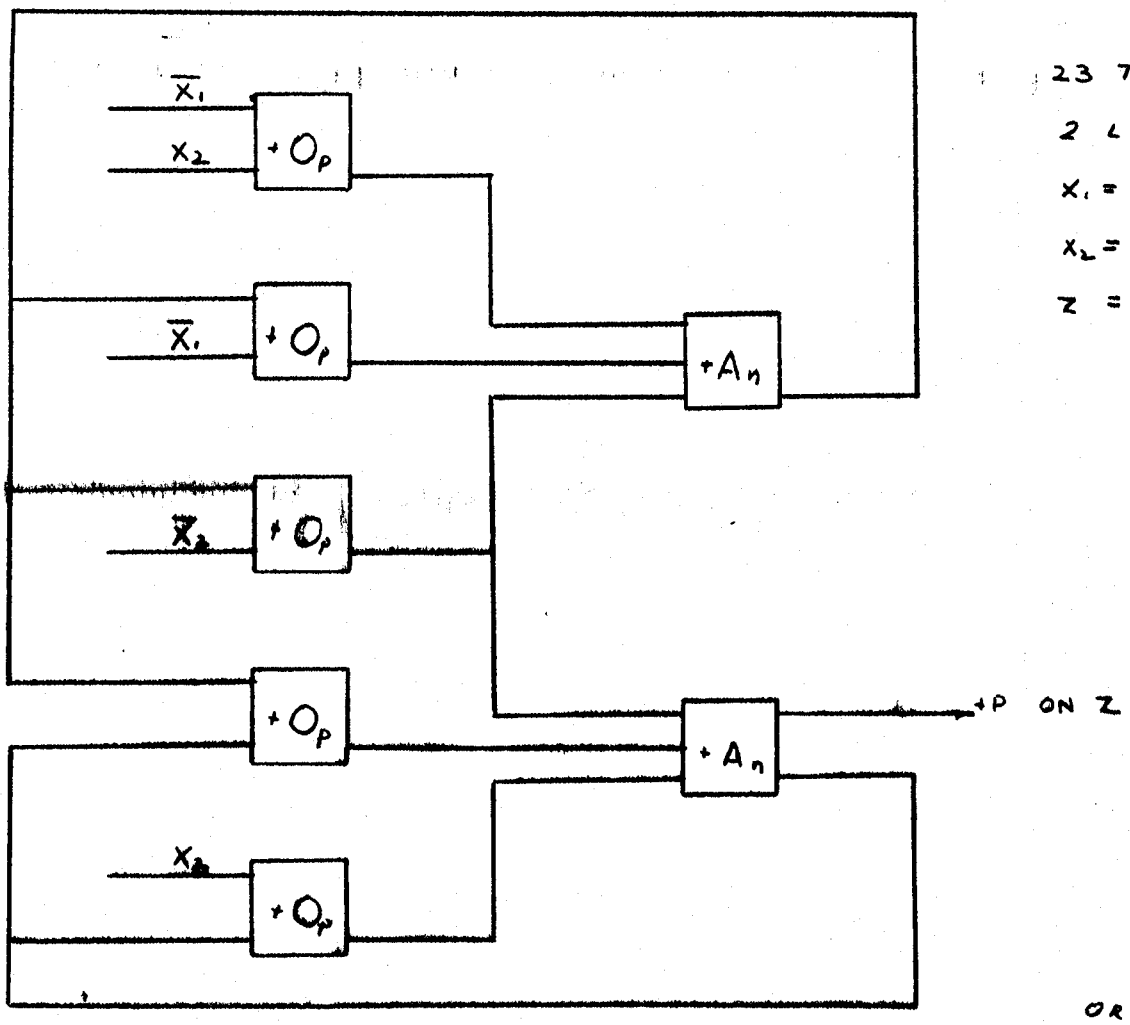
FIG 11

ESCAPEMENT GATE AND TRIGGER



15 TRANSISTORS
2 LEVELS
X_1 = DATA SIGNAL
X_2 = GATE SIGNAL
Z = OUTPUT

FIG 12



23 TRANSISTORS
2 LEVELS
X_1 = DATA SIGNAL
X_2 = GATE SIGNAL
Z = OUTPUT

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