21. Kolsky

SIGMA COMPUTER MEMO #4

SUBJECT: Memory Quantity and Addressing Requirements for Sigma System

BY: J. F. Dirac and R. J. Bahnsen

DATE: January 20, 1958

REFERENCE: Basic Computer Memo #3

Sigma Computer Memo #3

In the overall Sigma System,

1. Instruction "fetching" from memory

- 2. Operand "fetching" from memory
- 3. Indexing operations and
- 4. Execution operations

are planned to be overlapped. To permit this, it is necessary that conflicts in equipment usage be minimised. Sufficient equipment must also be available so that the system is "balanced" i.e., average rates for the four operations are equal. This prevents the auxiliary operations 1-3 from holding up the anticipated performance of execution without undue expense.

For example, consider two systems with different speeds of execution.

System I Average execution time of 1.5 us.

a. Equipment required:

Average execution or arithmetic time:

TA = 1.5us

Then the average indexing time must be at most:

TI = TA = 1.5us

Since two floating point instructions are contained in one instruction word, the instruction access time required is:

TDI = 3.0 us

This can be satisfied by one (1) 2.0 microsecond memory. Operands must be received from memory at a rate of one per 1.5 us. Two (2) 2.0 us memorys are needed to meet this rats. Therefore, memory requirements may be satisfied by one (1) 2,0 microsecond box containing instructions and two (2) 2.0 microsecond boxes containing operands.

b. Avoiding conflicts in equipment usage.

To accomplish this, it is desirable to store instructions in physical memory locations different than operands. This implies an addressing scheme identical to that anticipated in Basic Computer Memo #3 with sixteen (16) 0.5 microsecond memories. This would locate addresses 0 to 16,383 in Box I. Even addresses from 16, 384 to 65,534 would be located in Box 2. Odd addresses from 16, 385 to 65, 535 would be located in Box 3.

System II Average execution time of . 75 us

a. Equipment required:

With the same memory access times, the requirements are deduced as 2 boxes for instructions, 4 boxes for operands.

b. Avoiding conflicts in equipment usage implies the same alternative of boxes by address and function as described above.

> R& Bohnson R. J. Bahnsen

RJB: JFD: cts

J. H. Dirac