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BASIC COMPUTER MEMO #6

SUBJECT: Further Switch Matrix Considerations

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New relations have been discovered that necessitate a revision of the recommendations made in Basic Computer Memo #4, "Switch Matrix Considerations." In considering Designs I and II, the assumption has been made that the Register AB would simultaneously receive and transmit information in the ADD instruction. Since then, a control scheme has been suggested by Mr. John Hipp in which Register AB would transmit during the first part of a cycle and receive new data at the end of the cycle. We thus may consider two forms of control for Register AB as a whole.

(1) Simultaneous Receive - Transmit

(2) Sequential (Transmit then Receive)

If the simultaneous form of control is adopted, Switch Matrix Design I cannot be used, as may be seen in Figure 1.

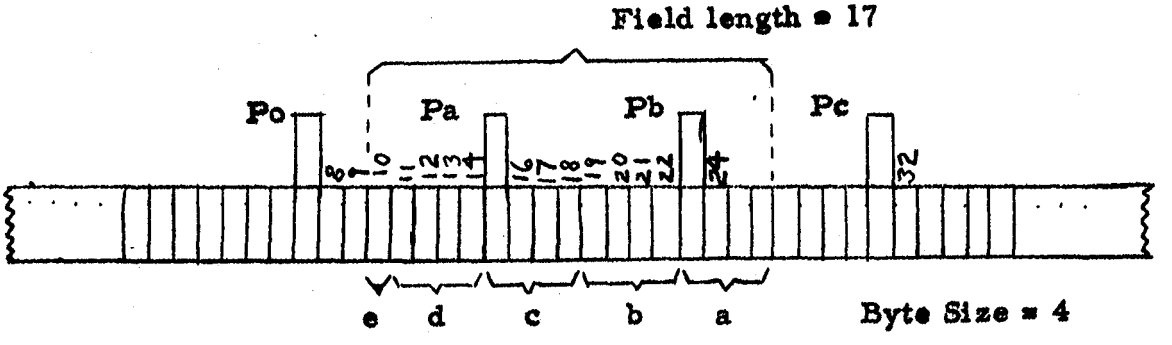

Figure 1. Example of Design I.

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The example uses a field address of 10, field length of 17, and byte size of 4. If the bytes are labeled a, b, c, d, and e, and there are five stages in the data-flow pipeline, then byte e is being transmitted while new results are being entered into the position of byte a. But according to Design I, if byte e is switched out then all the bits from address 8 through address 23 are selected by the Out Switch. The parity bits Pa and Pb are also selected. On the other hand, new results would be entered at the same time into addresses 23 through 26 and into the position of parity bit Pb. This means the register trigger at address 23 and the parity bit trigger Pb must, in general, simultaneously receive and transmit, which is not allowed.

Now considering the same example, but using Design II, we see that data bits from addresses zero (0) through 15 and parity bits Po and Pa are selected by the Out Switch whereas the bits at the position of byte a are receiving new results. There is no interference between transmission and reception of data.

Hence we may conclude that Design II must be used rather than Design I, if Register AB uses Simultaneous Receive-Transmit control. This is in spite of the relative simplicity of Design I.

If Sequential control is used, either scheme will work logically, since the interference will be prevented by the sequential control pulses rather than by logical arrangement of the Out Switch. Although Design I would appear more desirable, it is apt to be less reliable than Design II. Although a trigger may be able, logically, to transmit and receive data during the same cycle, to allow it to do so introduces the possibility of one more kind of error under marginal conditions.

It should be noted that whatever choice is made for the Out Switch of Register AB must also be made for the Out Switch of Register CD, since Register CD is the Accumulating Register for the ADD to MEMORY instruction.

In view of these further considerations and the current state of design work on the basic computer, Design II is felt to be the sounder choice at the present time.

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