Mr. J. C. Cooke

BASIC COMPUTER MEMO #3

SUBJECT: Addressing Scheme

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The following scheme, which is proposed for addressing memories with a continuous set of addresses, fulfills the requirement that there be no holes in the set and no loss in memory positions due to overlapping of addresses.

In order to accomplish said requirement, addresses will be assigned so that the .5 usec memory addresses start at zero and continue upward until all .5 usec memory positions have been addressed. The lowest position in 2 usec memory will be assigned an address one higher than the highest address assigned to .5 usec memory. The use of a set of addresses, for the 2 usec memories, which does not start at zero leads to a decoding problem. In order to overcome this problem, the CCU or Computer-Exchange will convert the set of addresses received for the 2 usec memory to a set of addresses which starts at zero. This second set will be obtained by the subtraction of the number of addresses assigned to .5 usec memory from each address which refers to a 2 usec. memory. The subtraction is to be done as part of the "memory frame decoding" in the CCU or Computer and Exchanges.

If the system is limited to the use of either 0, 1, 2, 4, 8 or 16, .5 usec memory boxes, both the identification of .5 usec or 2 usec addresses and the previously mentioned subtraction process become relatively simple to accomplish.

To determine whether an address refers to a .5 usec or a 2 usec memory, the high order bits of the address may be fed to an OR circuit.

If $\begin{Bmatrix} 0 \\ 1 \\ 2 \\ 4 \\ 8 \\ 16 \end{Bmatrix}$ .5 usec memory boxes are used, the bits in positions $\begin{Bmatrix} \text{none} \\ 11\text{-}18 \\ 12\text{-}18 \\ 13\text{-}18 \\ 14\text{-}18 \\ 15\text{-}18 \end{Bmatrix}$ of the address should be fed to the OR circuit. A one output from the OR circuit indicates an address in 2 usec memory, a zero indicates an address in .5 usec memory.

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For further treatment of the .5 usec addresses, the high order bits may be discarded. Then if {1, 2, 4, 8, 16} .5 usec memory boxes are used, the bits in positions {none, 1, 1 and 2, 1, 2 &3, 1, 2, 3 &4} may be used as .5 usec frame address. This use of the lowest bits will result in scanning (i.e. placing adjacent address in different memory frames to eliminate waiting for a memory to complete its operation before the next word may be read or written) and will leave 10 bits which may be sent to the appropriate memory frame as an array address.

If there are {1, 2, 4, 8, 16} .5 usec memory boxes, {2^{10}, 2^{11}, 2^{12}, 2^{13}, 2^{14}} must be subtracted from each address which refers to a 2 usec memory position.

The 10 lowest order bits will never be changed by the subtraction. If scanning is desired and if there are 1, 2, 4, 8 or 16 2 usec memory boxes, the appropriate number of lower order bits may be fed to the frame decoder without waiting for the results of the subtraction. If any other number of 2 usec memory boxes are used, the frame address must come (at least partially) from the highest order bits or holes will result.

The subtraction of 2^{11}, 2^{12}, 2^{13}, 2^{14} or 2^{15} may be accomplished with only two logical block delays. Figure 1 shows a logical circuit which will accomplish this. The subtraction will always be of the following form:

$$\begin{array}{r} \text{XXXXXXXXXXXXXX} \\ - \quad \underline{\qquad\qquad 10000000} \end{array}$$

Since the low order bits will never be changed by the subtraction, it may be reduced to the following form:

$$\begin{array}{r} \text{XXXXXX} \\ - \quad \underline{\qquad\quad 1} \end{array}$$

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It should now be noted that the lowest order bit will always be inverted. A higher order bit will be inverted only if all the bits lower than itself are zeros.

A translate block will be required to provide the proper level for the left input to the exclusive OR circuits.

The circuit will require about 100 transistors. Unless low order bits are used for frame addresses, the circuit will add about 30 musec to the time required for frame decoding in the CCU.

The circuit as shown is for subtracting 2^{11}, (i.e. 1,.5 usec memory box is being used). The switches shown can be used to change the circuit to accommodate other numbers of .5 usec boxes.

# .5 usec boxes	number to be subtracted	switches thrown
1	10000000000 = 2^{10}	none
2	100000000000 = 2^{11}	a
4	1000000000000 = 2^{12}	ab
8	10000000000000 = 2^{13}	abc
16	100000000000000 = 2^{14}	abcd
0	zero	abcde

If the registers in the basic computer are addressed as ≠ 0 to ≠ 63, the first 64 addresses in .5 usec memory or 2 usec memory if there are no .5 usec memories in the system, will be unavailable. These addresses could be made available by addressing the registers as — 0 to — 63. However, if the memory capacity were ever doubled by including negative addresses, it would probably be desirable to change the register addresses back to the positive set.

Disadvantages:

1. The system is limited to the use of 1, 2, 4, 8 or 16 .5 usec memory boxes. No other number of units could be used.

2. 30 musec might be added to the frame decode time in the CCU.

3. An additional 100 transistors would be required for each CCU input channel.

Advantages:

1. Memory is addressed with a continuous set of addresses for a large number of possible combinations of 0.5 and 2.0 us memory boxes.

2. Only 64 positions of memory are lost due to overlap. (No positions are lost if the registers are addressed with negative numbers.)

3. The .5 usec memories will be scanned without the use of additional equipment.

4. Decoding becomes straightforward and does not change as the number of .5 usec memories in use changes.

5. The subtraction circuit can be reasonably modified to accommodate 0, 1, 2, 4, 8 or 16 .5 usec memory boxes.

Examples:

I. There are no .5 usec memories and there are two (2) usec memories. All addresses will refer to 2 usec memories and there will be no modification.

Address

972 000 0 000011110011100

not used | 14 bit array address

frame adr.

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Address	
3,125	000 0 001100001101 01 (not used | frame adr. | 14 bit array adr.)
21,047	000 1 010010001101 11 (not used | frame adr. | 14 bit array adr.)

II. There are two .5 usec memories and four 2 usec memories. Bits 12-18 are used to test for .5 usec or 2 usec memory and 2 usec addresses are modified by subtracting 2^{11}.

Address	
972	test for 2 usec: 0000000 0111100110 0 (10 bit array adr. | frame adr.)
3,125	test for 2 usec: 0000001 10000110101
subtract 2^{11}	100000000000
modified adr.	000000010000110101 (not used | frame adr. | 14 bit array adr.)
21,047	test for 2 usec: 0001010010001101 11
subtract 2^{11}	100000000000
modified adr.	00 01 001010001101 11 (not used | frame adr. | 14 bit array adr.)

III. There are four .5 usec memories and eight 2 usec memories. Bits 13-18 are used to test for .5 usec or 2 usec memory and 2 usec addresses are modified by subtracting 2^{12}.

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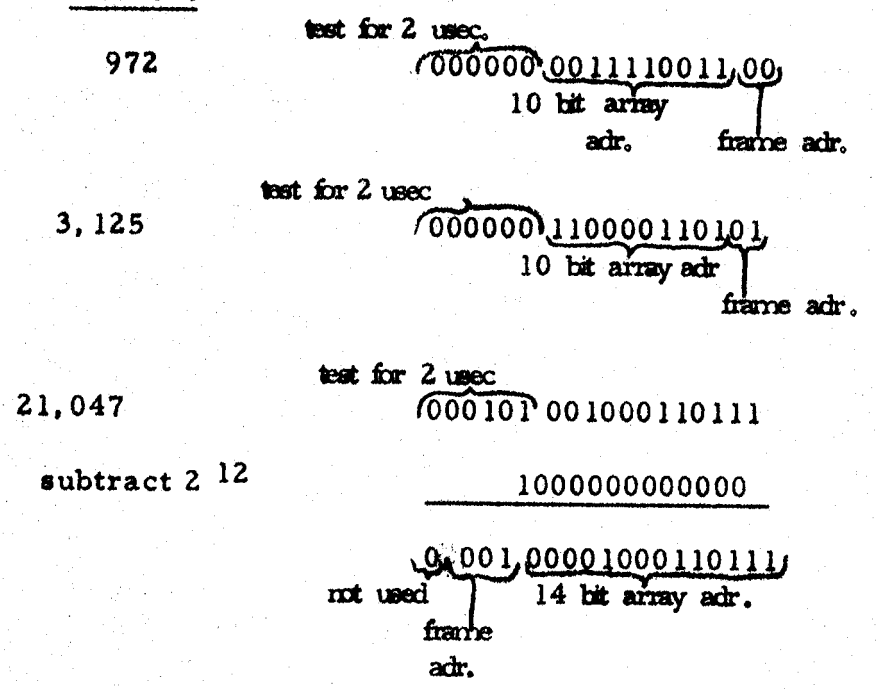
Address



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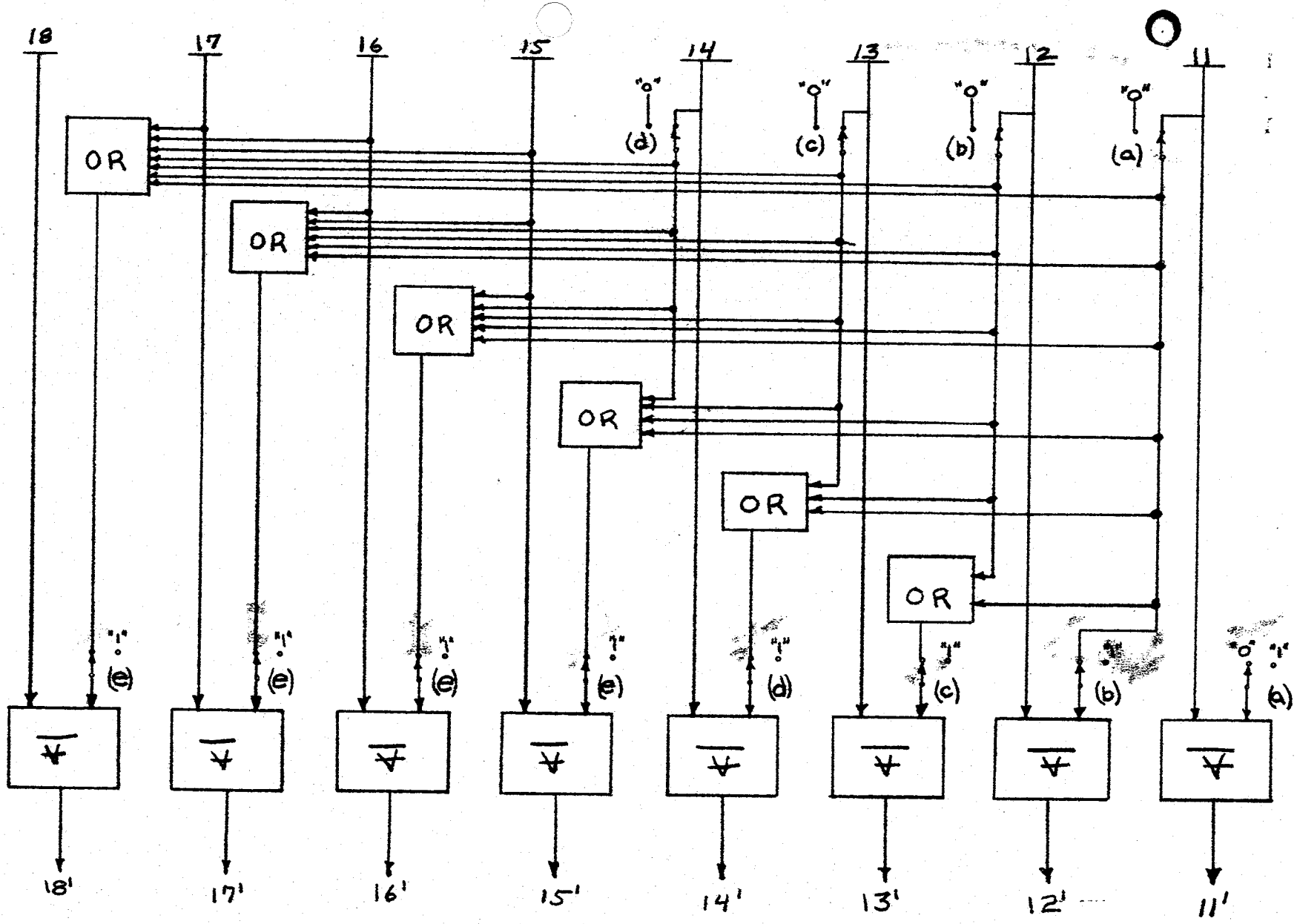

NOTE ~ THIS CIRCUIT IS DISCUSSED IN STRETCH FILE MEMO # 37.

FIG. 1

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