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SUBJECT: Preliminary Revised Chapter on Exchange

Attached is a preliminary revision of Chapter 2 of the Harvest Manual, which is intended to lead to a programmer's manual of the B-S-H system. Descriptive material and sections on the external units themselves have been omitted.

Also attached is a diagram showing the latest thinking on instruction and index word formats. The control word follows the index word format. It should be noted that the Class and Operation bits (9 bits) are currently undergoing further re-definition, but this does not affect the remaining format.

Please circulate your copy among your groups and bring any suggestions for changes to my attention.

W. Buchholz

WB/pkb

Encls.

1. Exchange and External Units

The function of the Exchange is to direct and control the information flow between many input-output units or external memory units on the one side, and the internal memory on the other side. In addition, the Exchange provides a number of common control facilities to be time-shared among the external units, thus keeping these units as simple as possible.

The basic Exchange permits up to 32 external units to be connected immediately to the system. These units are of the kind which operate serially, one byte at a time, at any reading or writing rate which does not exceed 67,000 bytes per second. A number of units may operate simultaneously through the Exchange, either reading or writing, the number depending on the speed.

High-speed tapes and disks follow the same philosophy of control as the basic Exchange, but separate equipment is required because the higher speed does not permit as much time-sharing.

A further extension of the basic Exchange is contemplated which will allow a great many more units of much lower speed to be accommodated simultaneously. Among these units will be manually operated devices and low-speed data links. Specifications for this section are not complete and it will not be provided initially.

The Exchange provides a general method of connecting many different kinds of units to a computing system. This will include direct input from remote sources, output to remote stations, communication with other computers which are not a direct part of the system, and input-output units using techniques still under development.

2. Instruction Control of External Units

The method of program control to be described in this section applies to all external units.

When instructions apply to external units, the computer executes all address modification. It then sends the addresses and the decoded operation to the Exchange, which completes the execution of the instruction by obtaining the operand (control word) from memory and starting the external unit. This procedure permits the Exchange, before it accepts an instruction, to determine from its stored status indication bits whether the unit is ready, and to sandwich into available time periods the extra cycles necessary to start an operation. If the unit is not ready (for instance, if the operator has stopped the unit manually for an indefinite time), the Exchange rejects the instruction and sends a signal to the program interrupt mechanism.

The computer waits until the Exchange has signalled that it has accepted or rejected the instruction. If the Exchange happens to be quite busy, the computer may have to wait some tens of microseconds because it is more flexible in its operation than most external units which cannot wait.

The computer ~~never~~ in many cases waits for the external unit to respond or to finish the operation, which may take milliseconds to minutes. The Exchange takes over full control and signals the computer when the operation is completed. The Exchange absorbs, only when timing is simple, not only regular starting delays and operating times, but it also waits for a tape unit to rewind or space over a block, for a printer to skip lines, etc., before initiating a new operation. Thus an instruction which has been accepted by the Exchange may remain in the Exchange for some time before the operation can actually begin.

The basic principle is that the Exchange can accept (only (not store)) an instruction from the computer just as soon as the previous operation for the same unit has been completed. This permits the computer program to continue without being held up by any delays which must be expected with external units. An instruction will be held, if necessary, while a tape unit is rewinding, etc. The Exchange cannot, however, accept more than one instruction for a given unit at a time. Any attempt to do this results in a program interruption.

3. Capacity of Basic Exchange

The Basic Exchange can accommodate 32 external unit controls or "adapters". With more than one unit per adapter, the number of units may go above 32.

Usually, each adapter serves one external unit, but some adapters may have two tape units attached, so that one can operate while the other is being rewound and loaded. Only one unit at a time is logically connected to its adapter and capable of responding to computer instructions; no two units connected to the same adapter can operate simultaneously. LOCATE instructions permit switching the adapter from one unit to another between operations.

The Basic Exchange permits a number of external units to read or write simultaneously, the number depending on the speed of each unit operating. The units are placed into three speed classes, each class having a "weight" attached to it:

Speed Class I - 60 microseconds per byte or slower - weight of 1.

Speed Class II - 30 to 60 microseconds per byte - weight of 2.

Speed Class III - 15 to 30 microsecends per byte - weight of 4.

The Exchange keeps a total of the weights of all units operating, and this total cannot exceed 32. If a read or write operation would result in the total exceeding 32, the Exchange rejects the instruction and gives an Exchange Busy indication. The instruction must be repeated at a later time after one or more currently operating units have disconnected.

Thus the Exchange can simultaneously accommodate:

32 units of Speed Class I,

or 16 units of Speed Class II,

or 8 units of Speed Class III,

or a suitable combination of fewer units of each class.

4. Reading and Writing

The basic reading and writing operation proceeds as follows: A READ or WRITE instruction is given by the program to initiate the operation. The instruction specifies the external unit and a "control word" location in memory. These two items are sent to the Exchange, and the computer program advances to the next instruction.

The Exchange then obtains from memory the control word which defines the beginning and end of the memory area to be used for reading or writing. The desired unit is then started and reading or writing proceeds until the entire memory area has been used, as indicated by the control word.

There are three variations of this operation:

(a) The external unit may terminate reading or writing if it reaches the end of a block before the entire memory defined by the control word has been used. READ and WRITE terminate by whichever of these two conditions happens first.

(b) If the instruction READ MULTIPLE or WRITE MULTIPLE is used instead of READ or WRITE, operation always continues until the specified memory area is exhausted. Thus more than one block may be read or written with one instruction. The only exception is if the external unit is stopped by some other condition, such as end of file.

(c) After the memory area defined by a control word is exhausted, it is possible for the Exchange to substitute another control word and continue, without stopping, in the memory defined by that control word. This feature, called "scatter-read" or "scatter-write" is described below.

5. Control Word

5.1 Data and Limit Addresses

READ and WRITE instructions include the address of a control word in memory to be used by the Exchange in executing the operation. The control word, as stored in memory, contains the address of the first data word in memory. Subsequent words are sent to consecutive higher memory addresses which the Exchange obtains by repeatedly adding one to the data word address in the control word. This continues until the Limit, specified in the control word, is reached.

The control word is stored during this operation in the Exchange itself, and the word as stored in main memory is left unchanged.

no subtraction?

Basically, the control word follows the same format as the index words used by all instructions. Thus the same word may serve as a control word while reading a block of data, as an address modifier giving the base address of the block while computing, and again, as a control word while writing that block.

The data word address is contained in the word address portion of the Value field. The Exchange ignores the bit address and sign portions of the Value field.

The word address portion of the Limit field determines the end of the data transfer (if it has not been terminated by other means, as explained below). The number of words transferred is then the difference between the word address in the Limit field and the initial data word address, ignoring signs and bit addresses. Thus the Limit is one word address higher than the last address actually used in memory.

The Exchange can only handle and address blocks of information starting at the left end of a full word in memory and containing an integral number of words (i.e., a multiple of 8 bytes). An external unit may, however, terminate operation at any time before the Limit address is reached. If, during reading, the last word has not been completed, the Exchange finishes the shifting process, filling in zero bits on the right of the last word, before sending the word to memory.

5.2 Control Word Interrogation

Normally, the Exchange operates with external units independently of the computer program, from the time the program initiates an operation until the time the Exchange signals to the computer the end of that operation, as described below. At that time, it is possible for the computer program to interrogate the control word to obtain more information.

EXTRACT CONTROL WORD

The instruction ~~TRANSMIT FROM EXCHANGE~~ specifies an external unit whose current control word is transmitted to the memory address also specified by the instruction. By the same procedure the program may at any other time, if desired for special procedures, monitor the progress of the operation.

The control word thus obtained contains information as to the status of the external unit and the operation performed. These "status bits" are placed by the Exchange in the 14 positions corresponding to the bit address and sign portions of the Value and Limit fields. The status bits are listed in a later section.

In addition, the control word will contain the next data word address to be used. All previous addresses are then known to have been used already and to be available for further operations, except that it must be realized that some kinds of errors are not detectable until the end of the block is reached.

5.3 Scatter-Read and Scatter-Write

Chain

The [illegible] bit in the index word defines whether one or more than one control word is to be used.

Chain

If the [illegible] bit is 0, the present control word is the last one.

Chain

If the [illegible] bit is 1, and the limit in the present control word has been reached, the Exchange automatically obtains another control word. To do this, each control word contains a Chain address which is the address of the next control word to be used. The last control word in the chain must contain a [illegible] bit of 0 to stop the operation, unless it is planned to have the external unit determine when to stop.

This technique is used to permit scattering of portions of a block of information in different areas of memory.

The scatter-read and scatter-write feature is not available with high-speed tapes and disks because of time limitations.

6. Instructions

The following 9 instructions are all that are needed to control any external unit regardless of speed. The computer and Exchange do not differentiate between different kinds of units which have different operating characteristics. The exact interpretation of how a unit responds to each instruction is a function of the design of the external unit, and will be described in connection with each unit.

6.1 READ
WRITE

These instructions initiate a reading or writing operation. The Second Address specifies the external unit and the effective Word Address specifies the first control word to be used. The control word, in turn, supplies the information defining the data addresses in memory. ~~Immediate addressing may not be used.~~

Information transfer is terminated either by a signal from an external unit or by the data address in the last control word reaching the specified limit, whichever happens first. If termination by limit occurs before the unit has reached the end of a block, the unit continues to the end by itself, independently of the Exchange, before permitting another operation to start. On reading, any partly filled word at the end of a block is completed automatically by filling the remainder of the word with zeros before storing it in memory.

6.2 READ MULTIPLE
WRITE MULTIPLE

These instructions are the same as READ and WRITE, except that information transfer is permitted to continue beyond the end of a block on the external unit. Information transfer is terminated when the last control word reaches its specified limit or when the external unit reaches the end of file or when an error occurs.

Each time the external unit signals the end of a block, a new word is started in memory. When reading, any remainder of the last word of each block is filled with zeros before storing it in memory and proceeding to the beginning of the next block.

6.3 CONTROL

The effective Word Address is sent as control information to the external unit specified by the Second Address.

The control information is decoded by the external unit to perform such functions as:

Rewind tape
Backspace tape
Space or skip on printer carriage
Turn on RESERVED light
Turn off RESERVED light

A single byte at the left end of the Word Address is sufficient to specify control for most units; the remainder is then ignored by the unit.

6.4 LOCATE

The effective Word Address is sent as an address to the external unit specified by the Second Address.

This instruction is used to set up external addresses on disk units, electronic printer-plotters, automatic tape cartridge changers, and similar devices. It is also used to select one of several units connected to a single unit adapter prior to the first time an instruction is given to that unit. Access to the specified location or unit is initiated, but the READ or WRITE instructions may follow at any time, whether access has been completed or not.

6.5 ~~DISCONNECT~~ RELEASE

The Exchange will accept a ~~DISCONNECT~~ RELEASE instruction while another ~~READ, WRITE, CONTROL, or LOCATE~~ instruction is still in progress for the external unit specified by the Second Address of the ~~DISCONNECT~~ RELEASE instruction. Any operation involving that unit is terminated immediately and the Exchange is released. The unit continues by itself to the end of its block. RELEASE also resets all status bits in the control word except Bit 56 (NOT READY).

This instruction permits the program to free Exchange and memory facilities when the program has determined that the external unit should not or cannot complete a transfer of information, ~~started by a READ or WRITE instruction.~~

6.6 EXTRACT CONTROL WORD

The current control word corresponding to the external unit specified by the Second Address is sent to the location specified by the effective Word Address. Bit addresses are ignored.

6.7 ENTER CONTROL WORD

This instruction is the same as READ (or WRITE) except that the unit is never started and no data are transferred. The Exchange merely sets up the control word specified by the effective Word Address in the Exchange memory location for the external unit specified by the Second Address. The status conditions controlling READ (or WRITE) also affect ENTER CONTROL WORD in the same way.

7. Status of External Unit

To permit the Exchange to control several external units, it must have available information as to the precise status of each unit. This information appears in the control word in bit positions 18 to 24 and 55 to 61, which correspond to the otherwise unused bit address and sign positions. The status bits are also available to the program on interrogation by means of EXTRACT CONTROL WORD.

The status bits have the following meaning:

Bit 18 - SELECT FOR READ
Bit 19 - SELECT FOR WRITE
Bit 20 - SELECT FOR READ MULTIPLE
Bit 21 - SELECT FOR WRITE MULTIPLE
Bit 22 - SELECT FOR CONTROL
Bit 23 - SELECT FOR LOCATE

These bits indicate that a corresponding operation is in progress for that unit.

Bit 24 - INTERRUPT WAITING

This bit indicates that an interrupt condition has not yet been sent to the computer.

Bit 55 - END OF MESSAGE

This is the normal signal indicating that an operation initiated for the unit has been successfully completed.

Bit 56 - UNIT NOT READY

The unit is not in a condition to be operated from the computer. This bit combines conditions such as: out of material, stacker full, operator stop, power off, control error, and mechanical malfunctioning.

Bit 57 - UNIT BUSY

The unit is in the process of executing an instruction previously given. This bit may remain on even after the Exchange has completed its part of the operation; e.g., the unit remains BUSY while it is rewinding (tape), spacing paper (printer), positioning the access mechanism (disk), etc. The Exchange will accept a new instruction under these circumstances, but the new operation is delayed until the unit ceases to be busy.

Bit 58 - END OF FILE
The unit has reached an end-of-file condition.

Bit 59 - CANCEL
The last operation initiated for the unit has been terminated without success. This status indication does not include data error. One use for this indication is with inquiry stations to permit an operator to wipe out a partial entry by means of a Cancel key. ~~This bit also comes on after a RELEASE instruction has been given to indicate completion of that operation.~~

Bit 60 - DATA ERROR
The last operation initiated for the unit has been terminated by a data error.

Bit 61 - OPERATOR SIGNAL
An operator's signal has been received from this unit. This signal has no functional significance. It is interpreted by programming, in whatever manner is desired, to establish communication between the operator attending a unit and the computer.

Bits 18 to 23 are the Select Status bits. They are turned on when the corresponding instruction is accepted. They are turned off when the operation is completed or when a ~~DISCONNECT~~ RELEASE instruction is given.

Bit 24 relates to delayed interrupts which are discussed in a later section.

Bit 55 is the normal end-of-message bit which comes on when an operation is completed. It is turned off automatically when the next operation is started. RELEASE also turns it off.

Bits 56 to 61 are the Exception Status bits. They come on when the corresponding condition arises. Bit 56 (UNIT NOT READY) can only be turned off by operator intervention to get the unit ready to operate. Bits 57 to 61 must be turned off by a RELEASE instruction. If any of the Exception Status bits are on, operation cannot proceed and subsequent instructions to operate the unit are rejected (see EXCEPTION REJECT, below).

8. Start of Operation

When the computer sends an instruction to the Exchange, the computer must wait a few microseconds until the Exchange has interrogated the status bits of the external unit and tested its own "weight" count to determine that it can accept the instruction. As soon as the Exchange signals the acceptance of the instruction, the computer proceeds normally.

If the Exchange rejects an instruction, one of three signals is sent to the program interrupt mechanism, turning on one of three indicators:

(a) EXCEPTION REJECT

An instruction was given for a unit which was not in condition to be operated. One of the Exception Status bits (Bits 56 to 61) in the control word is on.

(b) SELECT REJECT

An instruction was given for a unit which was still selected as a result of a previous instruction. One of the Select status bits (Bits 18 to 23) is on.

(c) EXCHANGE BUSY

An instruction was given which would cause the Exchange to exceed capacity, i.e., the total weight count would have gone above 32.

If the mask bit corresponding to these indicators in the interrupt mechanism has been set to 1, an interrupt takes place to permit the program to decide on a course of action.

If the mask bit for EXCEPTION REJECT or SELECT REJECT has been set to 0, the computer merely proceeds to the next instruction without taking any action.

If the mask bit for EXCHANGE BUSY has been set to 0, the computer waits until some other units disconnect and enable the Exchange to handle this traffic. The instruction is then completed. This special feature is provided to handle elementary situations, where the Exchange Busy condition would be a rare occurrence, without special programming.

9. End of Operation

When an operation concerning an external unit has been completed, the status at the end of the operation is recorded in the status bits of the corresponding control word, and the unit is disconnected.

If the operation has been successful, the END OF MESSAGE status bit (Bit 55) is turned on. It comes on when the information transfer has been completed on reading and writing, or when the required address or control information has been transmitted to the unit by a LOCATE or CONTROL instruction. When this bit comes on, the Exchange is finished with the unit, although the unit may remain busy for some additional time to do its part of certain operations independently of the Exchange.

If the operation is not successful, one of the Exception Status bits (Bits 56 to 61) is turned on. Again the Exchange is finished with the operation, but the program must take suitable action to take care of the special condition.

The External Interrupt Tag (XT) in the Control (Index) Word determines whether any of these conditions are permitted to cause a program interrupt. If XT = 0, no further signal is given. The program must test for any special conditions, either by interrogating the control word or by attempting a new instruction and looking for any instruction reject.

If XT = 1, one of two Indicators is set in the program interrupt mechanism, when one of the above bits comes on, and at the same time the external unit is stored in a unit address register in the computer. Bit 55 turns on the END OF MESSAGE indicator. Any one of bits 56 to 61 turns on the EXCEPTION indicator; here the program must interrogate the control word to discover which status bit is actually on. Once one of the indicators is turned on, program interrupt will occur subject to the standard masking and disabling provisions.

Interrogating the unit address register automatically resets the indicator and permits another external interrupt to occur. If an external interrupt condition occurs before the previous external interrupt has been reset, the Exchange turns on the INTERRUPT WAITING status bit (Bit 24). The interrupt will be presented at a later time when the previous one has been reset. Thus the computer deals with only one interrupt condition at a time.

10. Back-up Storage for Control Word

To permit the program to back up and re-read or re-write the last block with ease, provision has been made to store the initial control word for each unit in a separate location in the Exchange memory.

Every time a new block is started, the current control word is placed in this back-up storage. When multiple blocks are read or written with one instruction, this is done for every new block. If an error occurs, the unit stops at the end of the current block. After programmed or operator-controlled backspacing, it is possible then to re-start the block in error and to continue to the normal end if the error does not recur. To do this, the control word address in the read or write instruction is set to zero. A zero control word address is always interpreted by the Exchange to refer to the control word already stored there.

If desired, the instruction ENTER CONTROL WORD can be used to set up a control word in advance of a read or write instruction which must then have its control word address set to zero. This feature can also be used to read or write in the same memory area without repeating the access to the same control word in main memory.

(The back-up storage feature is not available for low-speed units which occupy special channels in addition to the basic 32.)

11. Initial Program Loading

When the power comes on, or when an Initial Load key on the Exchange is pressed, the Exchange will be set up to interpret the first Operator Signal in a special way.

The initial program can be loaded from any external unit. The operator, after readying the unit, presses its Operator Signal key. The Exchange automatically simulates a READ operation and a control word with

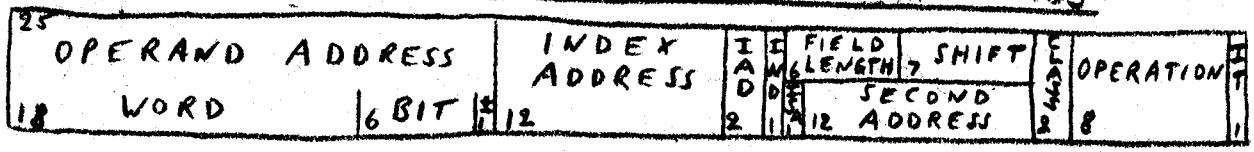
data address = 1 000 000 (decimal: 64)
limit = 1 000 100 (decimal: 68)

This causes 4 words to be read from this unit starting at address 64 in memory.

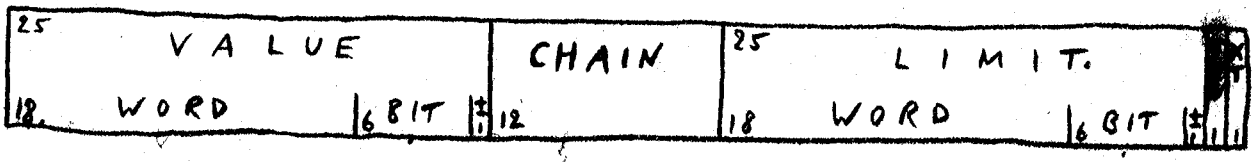
On a Start signal from the Exchange, the computer sets its Instruction Counter to 64 and starts program operation. The Exchange then reverts to the normal status, interpreting all subsequent Operator Signals in the normal way.

The initial program may consist of the instructions READ and BRANCH, followed by a control word to permit loading the next program block in any desired manner.

INSTRUCTION AND INDEX WORDS



INSTRUCTION WORD



INDEX WORD

Designators

IAD	Index Address Designator	00 Single 01 Advance 10 Multiple 11 Reset
IND	Indirect Operand Address	0 Direct 1 Indirect
ISA	Indirect Second Address	0 Direct 1 Indirect

Tags

IT	Instruction Interrupt Tag	0 No Interrupt 1 Permit Interrupt
XT	External Interrupt Tag	0 No Interrupt 1 Permit External Interrupt
CHN	Chain Tag	0 Last Word 1 Continue Chain

Classes

00 Binary VFL Arithmetic
01 Decimal VFL Arithmetic
10 Binary Floating Point
11 All Other Operations

Operation Bits

55 | 56 | 57 | 58 | 59 | 60 | 61 | 62

Class 00 }
Class 01 }
Class 10
Class 11

4 MODIFIERS	4 CODE BITS
3 MODIF.	5 CODE BITS
8 CODE BITS	

Operation Modifiers

Bit 55	0	Plus
	1	Minus
Bit 56	0	Signed
	1	Unsigned
Bit 57	0	Standard Byte Size (Class 00, 01) | Normalized (Class 10)
	1	Byte Size per Register (Class 00, 01) | Unnormalized (Class 10)
Bit 58	0	Normal Address
	1	Immediate Address

W. B. 7-19-57