May 10, 1957

MEMO TO: Mr. S. W. Dunwell

SUBJECT: Split Memory Cycles

I The possibility of operating the memory of a computer in two different modes has been proposed. These two modes may be described as "continuous" and "split".

The continuous memory cycle is defined as the cycle which is used at present in all magnetic core memories. Specifically, it is a cycle composed two subcycles, "Read" and "Write". In this cycle, the "Read" subcycle is always initiated first, followed immediately by a "Write" subcycle. This sequence is unalterable, and no provisions are made for independent operation of one of the subcycles.

The split memory cycle is nothing more than a provision for independent operation of the two subcycles. In other words, a Read subcycle may be initiated without an associated Write cycle, or vice versa. This arrangement has the advantage of requiring less time per cycle than the continuous cycle, In particular, the time will be approximately the same as the subcycle time of the continuous cycle. There are, however, some restrictions:

1. The Read subcycle, given independently, leaves the addressed word reset to all ones. This is destructive readout, and implies that the contents of the word are available only in the Memory Register.

2. The Write subcycle, given independently, will write only into a word which has been reset to all ones. Thus, a Write must follow a Read, as in the continuous cycle, but it may be given at a later time. If a Write is given with the address of a word which has not been set to all ones, the result will be the inclusive OR of the data to be written and the previous contents of the addressed word.

II If the split cycle can be used in programming, the memory time is effectively lessened by a factor of 1/2. If the number of references to a word of data in memory can be reduced by supplying certain special features (such as "prestore" and "poststore" commands) in a computer, the use of this cycle may be quite advantageous. This will reduce the time during which the memory is occupied by cycling, thus making the memory effectively available a larger proposition of the time. This means that the possibility of memory "conflicts" in an asynchronous machine is reduced and that more time will be available for I/O operations.

It is proposed that the split memory cycle be an adjunct to the continuous cycle, rather than a replacement for the continuous cycle. Thus, such a machine would have two different memory cycles available to the programmer, a continuous and a split cycle. It is presumed that the programmer could specify either cycle in any instruction which referred to memory. In fact, the arrangement is quite unsatisfactory under any other conditions.

It is also presumed that the continuous memory cycle will not be altered (lengthened) in the slightest degree by the provision for the split cycle. If the addition of a split cycle necessitates any lengthening of the continuous cycle, the proposal is self-defeating, for reasons stated later.

III Under the conditions stated in the previous section, several aspects of the use of the split memory cycle will be discussed.

A. Memory-to-Memory Data Transfers-In cases where a record or a group of words is transferred from one location in memory to another, such as working storage, the split cycle can be used to advantage. It will thus save about 1/2 of the total memory time, and it may speed up the operation of transferring the data, with a greater net gain of time.

B. I/O operations-The same technique is equally applicable to many I/O operations. Writing on tape, for instance, can be done in the split cycle mode for it is obvious that in most cases no further references will be made to the data. This mode could be very significant for high speed tape and disk file operations which occur at rates slightly slower than the memory access rate.

C. Checking-This subject points up a disadvantage in the use of split memory cycles. Suppose that during a problem, an error occurs and the program finds it necessary to back up to the beginning of the cycle in order to start the calculation over. If the split cycle had been used to read out the data, there would be no data left with which the cycle could be recalculated. Thus the programmer must be very careful when he uses the split memory cycle.

The same occurrence can happen when writing on tape. If a tape error occurs which requires that another attempt be made at writing the record from the beginning, it would be impossible if the split memory cycle had been used. Thus, it is also possible that the use of the split memory cycle is dangerous in certain I/O operations.

Nevertheless, it may be very useful in certain instances where the program is able, by other means, to correct errors. But this does not altogether account for the objection that, in the

general case, the use of the split memory cycle sacrifices certain restart procedures and its use will have to be carefully administrated by any programmer.

IV Returning now to the possibility of increasing the total memory cycle time in order to gain the split memory cycle in addition to the continuous cycle, it appears that the advantages may be outweighted in many cases by a new problem which is introduced by the split memory cycle-that of restart procedures. Restart procedures assume that a certain degree of permanence of the data exists. If the data happens to be a little less permanent than in the continuous cycle case, the restart procedures may be seriously impaired. Therefore, the time gained by the use of the split memory cycle may be lost in the restart procedure.

Thus, if the split memory cycle were acceptable on logical grounds (very debatable), it would not likely pay off enough in time gained to warrant the extension of the total memory cycle.

It seems, therefore, that the split memory cycle is useful only in certain special cases, and it should not be considered as anything but a secondary feature of memory design.

In other words, the split memory cycle is a weak addition to a computer for general purposes, and deserves a weak consideration for such purposes.

John Griffith

JG/jv