Automatic Program Interrupt Control

We shall, in the following, use the expression "break-in" to refer to the automatic interruption of a program under exceptional situations. In the STRETCH computer many new problems appear because of computer characteristics that have no precedent. For example, the asynchronous non sequential (hereinafter abbreviated as ANS) control allows the execution of control instructions prior to arithmetic operations which normally would precede them. Thus, the recording of enough information to permit continuation of a program after a stop occurs is made more complicated than in earlier computers where it is adequate to remember the last instruction executed for this purpose. In those situations where several operations are occurring simultaneously (e.g. computing and using input-output equipment) if break-in situations occur in more than one sequence of operations, some priority system appears to be necessary in order to determine the ordering of the corrective operations undertaken by the computer.

Break-in can occur in the following situations. This list is intended to be representative only and is far from being complete.

1. Exceptional results or operands in floating point operations.

2. A divisor which does not exceed in absolute value the dividend in a fixed point division.

3. An error in reading or writing some input-output device.

4. An error in an arithmetic operation.

5. An error in the registration of a word in one of the high speed memories.

The above situations are not anticipated by the programmer. It may also be desirable to use automatic break-in types of transfer in the following situations.

6. Passing control from the SIGMA computer to a DELTA computer, or vice versa.

7. Tracing.

8. Passing control to and from subroutines.

It may be thought desirable to make the corrective actions for (3), (4), (5) completely automatic, while the programmer can exercise arbitrary control in (1), (2). However, it is our opinion at this writing that it is preferable to handle all of these situations by programmed control. There seems to be little advantage in making the response to (3), (4), (5) completely automatic because this is likely to increase significantly the complexity of the hardware and these situations should occur so rarely that little machine time would be lost by requiring specially programmed action. It is probably desirable in these situations to record more information (location and type of error) for diagnostic purposes than could be easily gotten with additional circuitry.

It is assumed that a "Mask Word" will be under the control of the programmer. The 64 bits of this word will refer to the status of as many "triggers" which respond to various machine states (exponent overflow, error detecting bit inconsistencies, etc.). In addition, an "Indicator Word" will indicate the present status of these triggers. When the logical product of these words is other than zero a break-in will occur.

The five ANS control registers (or decoder) will be duplicated in five reserved memory registers as the first step in the break-in procedure. It will probably be desirable that the break-in procedure be informed of the locations of the instructions in the decoder and it is therefore suggested that these locations appear in the decoder registers as well as the instructions themselves.

In all operations parallel to those in the central control unit it is assumed that the device exterior to the control frame will be given a command and then will, on its own, proceed with the execution of this command until its completion. A trigger will be set simultaneously with the issuing of the command by the central computer and will be released by the actuating device upon the completion of its task. (The device may be an input-output unit or a delta computer). If a break-in occurs because of some situation in the use of the auxiliary unit, control will be transferred to a program-interrupt device which will halt the program in the main control unit (unless the program has already been halted by a previous break-in). It will be the responsibility of the programmer to test that the auxiliary units have correctly completed their assigned tasks before continuing with the program.

If a second break-in occurs while correcting a prior break-in situation no special difficulties are encountered. The programmed corrective action will have recorded the status of the various parts of the machine at the time of the first break-in which are necessary to the continuation of the program from that point and return to this point can be effected after handling the most recent break-in. It will be the responsibility of the break-in program to "remember" the Indicator Word contents, the contents of the ANS control registers and whatever other information is necessary to continue the interrupted program for each break-in.

The writing of the special instructions needed to handle all the complexities of compound break-ins may not be such a chore because it seems possible to write a library program that would accomplish most of this and it could automatically be included in all programs.

A special SUBROUTINE instruction has been suggested by Mr. W. P. Heising. This instruction located at A would contain addresses B and C. It would cause the program to transfer to B and continue with the subroutine beginning at this location until an instruction from location C is called for. When this occurs the program would automatically revert to the instruction at A + 1. If the instruction SUBROUTINE is given before the return transfer for a preceding SUBROUTINE instruction has been effected, the machine would remember enough information to permit this return to occur after execution of the present instruction and return to the location following it. This would all be accomplished by additional hardware including a "compare address register", a "comparator", "subroutine level counter" and "subroutine level keyword storage".

Thus, this type of instruction is a modified break-in. However, to handle it in the same way as the preceding described break-in would involve substantially more hardware. It would be necessary to set up a selector, when the instruction SUBROUTINE is given, which would be turned ON when the number appearing in the instruction location counter becomes equal to the number C appearing in one of the address fields of the instruction. It, at this time, seems to be worthy of inclusion in the break-in system.

We summarize below the steps involved in the break-in system.

1. The programmer shall be able, by means of special instructions, to set up the contents of a "Mask Word" register. As a result of a SUBROUTINE instruction one of the bits in this word will indicate the status of a "trigger" which is turned ON when the contents of the instruction counter become equal to an address mentioned in the SUBROUTINE instruction. A limited number of bits in the "Mask Word" will be available for this purpose. The particular bit used for a given SUBROUTINE instruction is "remembered" and if another such instruction appears in the program the succeeding bit will be used as its trigger. A bit is "released" and available for use by other SUBROUTINE orders when the return transfer occurs. At the time of execution of the SUBROUTINE instruction, fixed locations in fast memory corresponding to the trigger positions are loaded with the A+ 1 location for return control and the C location which indicates the end of the routine. All of this can be done automatically by hardware, but it is our feeling at this time that it can be largely accomplished by the library program referred to above, without significant loss of machine time.

2. When a break-in occurs transfer will be made to a fixed location in the machine which is the beginning of a library routine that will always be incorporated into programs.

3. The first action of the library program will be to "copy" the contents of the ANS control registers. Special hardware will have to be included in order to permit this. Under optional control, the program will also save the contents of all arithmetic and control registers to permit normal resumption of the program at the conclusion of the break-in.

4. This program will detect the bit (or bits) that appear in the logical product of the mask word and indicator word. A transfer will be made using indirect addressing to the contents of a location corresponding to this bit (if there is more than one only one will be handled at a time). Some of these transfers will be automatically made by the library program. In some cases the programmer can exercise the option of changing a transfer address.

5. The library program will record the frequency and location of machine errors, occurrence of overflows and underflows, etc. if desired.