EXCHANGE

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PROJECT STRETCH

Exchange Machine Definition

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1 GENERAL SPECIFICATIONS

The specifications which must be met by the Exchange are directly related to the operational characteristics of the Delta system. The system employs a core memory the word size of which is 72 bits, of which 64 are data and 8 are error detection and correction information. The memory cycle is 2 microseconds. Execution of instructions by the computer is accomplished at a speed which is comparable to the speed of the memory. A salient feature of the system is the ability to simultaneously Read, Write, and Compute.

The Exchange provides the facility for data word transfer between the main memory of the computer and the peripheral bulk storage and I/O units. It also transmits control information to the peripheral units and monitors their operation.

1.1 The Basic Exchange accommodates devices which operate on a serial by byte basis with 8 bits per byte. The devices are connected to the Exchange through a magnetic core crosspoint switch. Sixty-four medium speed input/output devices can be connected permanently to the Exchange through the crosspoint switch. Any 8 of these devices may be operated simultaneously. Storage is provided within the Exchange for a data word and a control word associated with each unit.

1.2 The types of units accommodated by the Basic Exchange include:

a. Card Readers
b. Punches
c. Printers
d. Direct Access Disks
e. Communications Tape (727 type)
f. Document Readers

1.3 Data is transferred between the main memory of the Computer and the Exchange on a full word basis. The full word consists of data bits and ECC (Error Correcting Code) bits. There will be 64 data bits and probably 8 ECC bits.

1.4 Data is transferred between the Basic Exchange and the I/O devices serial by byte. Each byte consists of 8 bits plus one parity bit.

On Reading, the Basic Exchange assembles the incoming 8-bit bytes into full words using the data word storage provision for partial word storage. When a full word is completed, it is transferred to the main memory at the address specified by the associated control word.

On Writing, the Basic Exchange obtains the data words to be written from the main memory at the address specified by the associated control word. The data words are broken up into 8-bit bytes which are sent to the selected output unit.

1.5 Each input or output device will contain such individual control circuitry and data handling circuitry which is unique to the device and cannot be reasonably included as common to all input or output devices in the logical organization of the Exchange. Specifically such circuitry which is necessary to allow simultaneous operation of several input-output devices would be included in this category. The necessary circuitry to allow packing of the data into 8-bit bytes for input units and utilization of packed 8-bit bytes by output units are also included in the input-output control circuitry.

1.6 After the initial instructions for reading from or writing to a selected unit is given, together with the initial memory address of the first word in the block and the number of words in the block, the Exchange executes the instruction and monitors its operation until complete with no further control by the Computer.

1.7 Extensions of the Basic Exchange.

Additional sections of equipment can be added to the Basic Exchange to provide the facility to accommodate devices which differ from the devices limited in section 1.2 either because of much greater or much lower information rates or because the mode of operation is inherently different.

1.7.1 Low Speed Channels.

One input and one output channel may be added to accommodate up to 256 low speed devices and inquiry stations. The system will be able to accommodate simultaneous operation of all 256 units.

1.7.2 Another extension of the Basic Exchange will be four input/output channels to allow simultaneous operation of four X10 type tape units.

1.7.3 If both 1.7.1 and 1.7.2 are desired, the operation in section 1.7.2 must presently be restricted to two X10 tape units.

2.0 MACHINE OPERATION

2.1 GENERAL

The basic purpose of the Exchange is to control the transfer of information between the external input-output devices and the main memory which is common to both the Exchange and the Computer.

Operation of the Exchange is under control of the Computer where the initial decoding of instructions is done. If an instruction pertains to an input-output device, the Computer sends the instruction to the Exchange, after which the Computer is free to go on to the next instruction. The Exchange does the final interpretation and execution of the instruction independently of the Computer.

2.2 INSTRUCTIONS

The format of each instruction sent to the Exchange is listed below along with a brief description of the instruction.

2.2.1 WRITE INSTRUCTION

The write instruction transfers data from main memory to an output unit. The format of the instruction sent to the Exchange is:

a)	1 bit	Write
b)	9 bits	I/O unit address
c)	20 bits	Control word address

2.2.2 READ INSTRUCTION

The read instruction transfers data from an input unit to main memory. The format of the instruction sent to the Exchange is:

a)	1 bit	Read
b)	9 bits	I/O unit address
c)	20 bits	Control word address

2.2.3 INTERROGATE I/O UNIT STATUS INSTRUCTION

This instruction transfers the status of an I/O unit from exchange memory to the Exchange is:

a)	1 bit	Interrogate I/O unit status
b)	9 bits	I/O unit address

2.2.4 COPY CONTROL WORD INSTRUCTION

This instruction transfers an I/O unit's control word from exchange memory to main memory. The format of the instruction sent to the Exchange is:

a)	1 bit	Copy control word
b)	9 bits	I/O unit address
c)	20 bits	Control word address

2.2.5 CONTROL I/O UNIT INSTRUCTION

This instruction transfers control data from main memory to an I/O unit. The control data is interpreted as a control instruction by the I/O unit. The control I/O unit instruction sent to the Exchange can have either of two formats. If the control data is no more than 20 bits, it is part of the instruction word and the format is:

a)	1 bit	Control I/O unit
b)	1 bit	Control word address is data
c)	9 bits	I/O unit address
d)	20 bits	Control data

If the control data is more than 20 bits, it is not part of the instruction word and the format is:

a)	1 bit	Control I/O unit
b)	9 bits	I/O unit address
c)	20 bits	Control word address

2.3 EXCHANGE COMPONENTS AND FEATURES

To execute the above instructions, the Exchange contains the following components and features.

2.3.1 EXCHANGE MEMORY

The exchange memory is a 1 micro-second core memory. The word length is 79 bits. The memory is divided into two sections; one for data words and one for control words. Each input-output unit has a particular data word location and a particular control word location associated with it. The data word address is the same as the input-output unit address. The control word address is the input-output unit address plus the high order address bit.

2.3.2 DATA WORD

The format of the data word stored in the exchange memory is as follows:

a)	data	64 bits
b)	check information	8 bits
c)	byte count	4 bits
d)	select for read flag	1 bit
e)	select for write flag	1 bit
f)	select for control flag	1 bit

Only the data and check information (72 bits) are transferred between the exchange memory and the main memory. The remaining bits are inserted by the Exchange.

a) Data - When reading, the 64 bits of data are received from the input unit a byte (8 bits) at a time. Each time a byte is received the unit's data word is read from exchange memory and shifted left 8 bit positions. The byte is inserted into the right end of the data word and the data word is written back into exchange memory cycle. When a full data word has been assembled from the input unit the 64 bits of data and the 8 checking bits are transferred to main memory.

When writing, the 64 bits of data and the 8 checking bits are transferred from main memory and stored in exchange memory at the data word address of the unit. Each time the output unit requires data, its data word is read from exchange memory and the left byte (8 bits) are sent to the unit. The data word is shifted left 8 bit positions and written back into exchange memory during the same memory cycle. When the data word in exchange memory is empty, a new data word is obtained from main memory.

From the above description it can be seen that each data word storage in conjunction with the exchange memory word register and shifting circuitry is in effect a shifting register for its associated input-output unit.

b) Checking Information - The 8 bits of checking information consist of 8 error correcting code (ECC) bits. These 8 bits provide single error correction and double error detection. A more detailed explanation of checking is given later.

c) Byte Count - When reading, it is necessary to sense when a full data word has been assembled from an input unit. This is done by examining the byte count which is stored with each data word. An initial byte count is stored in the byte count section of the data word before receiving the first input byte. Each time that the data word is read out of exchange memory and a new byte added to it the byte count is stepped

minus one. When the byte count is zero the 72 bit data word is sent to main memory under control of the control word.

When writing, it is necessary to sense when a complete data word has been sent to an output unit. This is done by storing an initial byte count in the byte count section of the data word before sending the first byte to the output unit. Each time that the data word is read out of exchange memory and a byte is removed and sent to the output unit, the byte count is stepped minus one. When the byte count is zero, a new data word is obtained from the main memory under control of the control word.

d) Select for Read Flag - When an input unit which is connected to either the byte or word crosspoint switch is selected for reading, a select for read flag bit is stored in the unit's data word until an input channel is assigned to the unit. If a channel is immediately available when the instruction is given the flag bit is not stored in the data word.

For low speed units that are connected to the Exchange via the low speed channels, the select for read flag bit serves as a method of selection as explained in section 2.4.

e) Select for Write Flag - When an output unit which is connected to either the byte or word crosspoint switch is selected for writing, a select for write flag bit is stored in the unit's data word until an output channel is assigned to the unit. If a channel is available when the instruction is given, the flag bit is not stored in the data word.

f) Select for Control Flag - When an input or output unit which is connected to the Exchange via a crosspoint switch is selected for control, a select for control flag is stored in the unit's data word until an output channel is assigned to the unit.

For low speed units that are connected to the Exchange via the low speed channels the select for control flag bit serves as a method of selection as explained in section 2.4.

2.3.3 CONTROL WORD

The control word contains the information necessary for the Exchange to control the operation of an input-output unit independently of the Computer. A control word in exchange memory contains the following information:

a)	control word address	20 bits
b)	word count	15 bits
c)	data word address	20 bits
d)	grouping/distribution flag	1 bit
e)	ECC Indicator	1 bit

f)	check information	8 bits
g)	unit status	8 bits

a) Control Word Address - When reading the control word address is used in conjunction with the grouping/distribution flag for distributing successive sections of a record read from an input unit to various blocks in main memory. When writing the control word address is used in conjunction with the grouping/distribution flag for grouping various blocks of data contained in main memory into one record at the output unit. Each block requires a new control word from main memory. The control word address specifies the main memory address of this new control word.

b) Word Count - When reading, the word count specifies the number of words to be read from the input unit. As each word is transferred to main memory the word count is decreased by one. Reading from the input unit is ended when the word count reaches zero and there is no grouping/distribution flag or when the end of record is reached in the input unit, which ever occurs first.

When writing, the word count specifies the number of words to be sent to the output unit. As each word is transferred from main memory, the word count is decreased by one. Writing to the output unit is ended when the word count reaches zero and there is no grouping/distribution flag bit or when an end of message signal is received from the output unit.

c) Data Word Address - The data word address specifies the main memory address when a data word is transferred from or to main memory. The data word address is increased by one each time a data word is transferred between the Exchange and main memory.

d) Grouping/Distribution Flag - The grouping/distribution flag signals the Exchange to obtain a new control word from main memory when the word count reaches zero. The address of the new control word is specified by the control word address. The last control word used in reading or writing a record should not contain a grouping/distribution flag, thus allowing the read or write operations to end.

e) ECC Indicator - When writing, the ECC Indicator signals the Exchange to send the 8 ECC bits contained in each data word to the output unit. If there is no ECC Indicator, the 8 ECC bits are discarded and only the 64 information bits in each data word are sent to the output unit.

f) Check Information - The 8 checking bits consist of 8 error correcting code (ECC) bits.

g) Unit Status - The following eight bits represent the status of the input-output unit and are sent to the Computer when an instruction is rejected, in response to an interrogate I/O unit status instruction and when an end of message signal is sent to the Computer.

1) I/O Unit Not Ready - Indicates that the unit is not mechanically ready.

2) I/O Unit Busy - Indicates that the unit is still busy as the result of a previous instruction.

3) I/O Unit at End of File - Indicates that the unit has reached the end of tape, etc.

4) I/O Unit R/W Error - Indicates that the unit had made a read or write error.

5) I/O Data Transmission Error - Indicates a data error was detected between the input unit and the input register or between the output register and the output unit.

6) Exchange Data Handling Error - Indicates the data word is incorrect in the Exchange.

7) Control Circuits Error - Indicates errors such as no service request from the unit, etc. Anything attributable to the malfunction of control equipment.

8) Exchange Control Word Error - Indicates the control word is incorrect in the Exchange.

2.3.4 MAGNETIC CORE CROSSPOINT SWITCH

The magnetic core crosspoint switch provides for permanently connecting up to 64 medium speed input-output units to the Exchange. The crosspoint switch provides the facility for connecting any one of the 64 units to any one of 8 input or 8 output channels, thereby providing an information and control path between the input-output unit and the Exchange. Any 8 of the input-output units may be operated simultaneously.

The crosspoint switch is divided into an input section which contains 8 input channels and an output section which contains 8 output channels. Units that can read and write are connected to the input crosspoint switch and the output crosspoint switch. Units that can write only are connected to the output crosspoint switch. Units that can read only are connected to both switches, since control instructions are sent to the units via the output crosspoint switch.

The two crosspoint switches are 8 by 64 matrices. At the intersections are multihole ferrite cores. These cores have the property that storage is possible only when they are in a selected state resulting from a particular flux configuration. An intersection (core) is selected by coincident current on a column and a row. The crosspoint cores in a column are common to a particular channel; the crosspoint cores in a row are common to a particular input-output unit.

2.3.5 CHANNEL ASSIGNMENT

The instructions Read, Write or Control require that a channel be assigned to an input-output unit. If the instruction is Read, an input channel is assigned to this unit; if the instruction is Write or Control, an output channel is assigned to the unit.

The input-output unit is determined by decoding the I/O unit address register. The channel is determined by circuits in the Exchange which indicate the next available input channel and output channel.

If a channel is not available when the instruction is received from the Computer the control word is transferred from main memory and a select flag bit (either Read, Write or Control) is stored in the unit's data word. When a channel becomes available it is assigned to the unit and the select flag is removed from the unit's data word.

An available channel is assigned to an input-output unit by putting half current on the vertical channel line and half current on the horizontal line common to the unit. The unit is specified by the I/O unit address register. The crosspoint at the intersection of the two currents is turned on, thus providing an information and control path between the unit and the Exchange . The selected crosspoint core is also a buffer register between the unit and the Exchange.

2.3.6 CHANNEL SERVICING

a) Input Channels - Each input channel contains the following:

1) Available Trigger - This trigger is on when the channel is available and off when it is busy.

2) Address Register - The address register contains the address of the unit connected to the channel. When the channel is serviced, this register determines the exchange memory address.

3) Service Request Trigger - When the unit sets a byte into the crosspoint core it also turns on the channel service request trigger to indicate to the Exchange that the channel contains a byte of data and therefore requires servicing.

4) Control Word Modification Trigger - This trigger is turned on by the Exchange when a complete data word has been assembled from the unit. The on condition of this trigger signals the Exchange to modify the control word and to transfer the full data word to main memory.

5) Read Amplifiers (9) - Amplifies the signals received from the crosspoint cores in that channel.

6) New Control Word Trigger - This trigger is turned on by the Exchange if the word count reaches zero and the control word contains a distribution flag bit. The on condition of this trigger indicates to the Exchange that a new control word should be obtained.

7) End of Message Trigger - This trigger is turned on by the unit when it reaches the end of message.

8) End of File Trigger - This trigger is turned on by the unit to indicate that it has reached the end of file.

9) Error Trigger - This trigger is turned on by the unit to indicate that the byte being sent is in error.

After a channel is assigned to a unit a start signal is sent to the unit. When the unit receives the start signal, it proceeds to get up to speed or to otherwise search for the first information contained in the record. When the unit reads the first byte, it sends the byte into the input crosspoint switch along with a service request signal. The byte consists of 8 information bits and a parity bit. The circuits at the input crosspoint switch attempt to write the byte into all crosspoint cores common to the unit, but only the selected core stores the byte. The service request signal also passes along the horizontal line common to the unit, but only the selected core passes the signal up the channel to turn on the channel service request trigger.

A channel scanning device is continually scanning the channel service request triggers and stops on the channel whose service request trigger is on. The Exchange services the channel marked by the channel scanner. If more than one service request trigger is on, the channels are serviced in sequence.

To service an input channel, the Exchange executes a 1 microsecond input data subcycle. During an input data subcycle the Exchange:

1) Reads the unit's data word from exchange memory. The address of this data word is the address of the unit which is contained in the channel address register.

2) Shifts the data word left 8 bit positions.

3) Reads the byte from the crosspoint core into the input byte register.

4) Steps the byte count - 1.

5) Writes the data word back into exchange memory. (The input byte register conditions the right 8 bit positions of the data word).

6) Turns off the channel service request trigger.

During the above cycle, 8 bits are added to the data word. The input unit sets another byte into the crosspoint core in approximately 40 microseconds. In the meantime, the Exchange is servicing other channels. Each time the unit sets a byte into the crosspoint core, it turns on the channel service request trigger signalling the Exchange to execute an input data subcycle to service that channel.

b) Output channels - Each output channel contains the following. Note that an output channel is similar to an input channel except that the information flow is in the opposite direction.

1) Available trigger - This trigger is on when the channel is available and off when it is busy.

2) Address Register - The address register contains the address of the unit connected to the channel. When the channel is serviced, this register determines the exchange memory address.

3) Service Request Trigger - When the unit removes a byte from the crosspoint core, it also turns on the channel service request trigger to indicate to the Exchange that the channel requires servicing.

4) Control Word Modification Trigger - This trigger is turned on by the Exchange when a complete data word has been sent to the output unit. The on condition of this trigger signals the Exchange to modify the control word and to transfer a data word from main memory to the Exchange.

5) Write Drivers (9) - Writes the byte contained in the output byte register into the crosspoint core.

6) New Control Word Trigger - This trigger is turned on by the Exchange when the word count reaches zero and the control word contains a grouping flag bit. The on condition of this trigger indicates to the Exchange that a new control word should be obtained from main memory.

7) End of Message Trigger - This trigger is turned on by the unit to indicate that it has reached the end of the message.

8) End of File Trigger - This trigger is turned on by the unit to indicate that it has reached the end of file.

9) Error Trigger - This trigger is turned on by the unit to indicate that the byte received is in error.

After an output channel is assigned to a unit, a start signal is sent to the unit. The output unit sends back a service request signal in response to the start signal. This service request turns on the channel service request trigger, indicating to the Exchange that the channel requires servicing.

The on condition of the service request trigger causes the channel scanner to stop on this channel and the Exchange executes a 1 microsecond output data subcycle to service this channel. During the output data subcycle, the Exchange:

1) Reads the unit's data word from the exchange memory. The data word address is the same as the address of the unit. This address was set into the channel address register when the channel was assigned to the unit.

2) Sets the left 8 bits of the data word into the output byte register.

3) Generates a parity bit for the above 8 bits and sets it into the output byte register.

4) The nine channel write drivers, which are conditioned by the output byte register, send write current through all the cores common to the channel, but only the selected core stores the byte.

5) Steps the subcycle count - 1.

6) Shifts the data word left 8 bit positions.

7) Writes the data word back into exchange memory. (It no longer contains the 8 bits sent to the output unit.)

8) Turns off the service request trigger, which causes the scanner to move to the next channel that requires service. The turning off of the service request trigger also generates a "character available" signal, to the output unit. This signal is used by output devices which do not operate on a fixed information rate, but can accept bytes as fast as the Exchange can supply them.

2.3.7 CONTROL WORD MODIFICATION

Each time a data word is to be transferred between the main memory and the Exchange, its associated control word is first read from exchange memory. The control word is read from exchange memory, modified and written back during a 1 microsecond control word modification cycle. During a control word modification cycle, the Exchange:

1) Reads the control word from exchange memory.

2) Sets the data word address into the main memory address register. This register specifies the main memory address when a word is transferred between main memory and the Exchange.

3) Steps the data word address + 1. The device used for advancing the data word address is essentially a simplified parallel adder with one set of inputs and special carry circuits to minimize carry propogation time.

4) Steps the word count - 1. The device used for decreasing the word count is a simplified parallel subtracter with one set of inputs and special carry circuits to minimize carry propogation time.

5) Writes the modified control word back into xchange memory.

Following the control word modification cycle, the associated data word is transferred to or from main memory. The modification of the control word and the transfer of the data word require that the Exchange dwell on the channel for a 2 microsecond period, which is the maximum time that the Exchange ever dwells on a channel.

2.3.8 OBTAINING A NEW CONTROL WORD

If the word count reaches zero and the control word contains a grouping/distribution flag bit, a new control word is obtained from main memory. Operation of the input/output unit is not interrupted.

The new control word is not obtained immediately, but instead the channel "new control word" trigger is turned on to remember that the channel (actually I/O unit) requires a new control word. The Exchange then advances to other channels that require servicing. After all channels have been serviced, the channel scanner scans the channel "new control word" triggers. The on condition of a "new control word" trigger causes the Exchange to stop on the channel and read the associated control word from exchange memory. The control word address is set into the main memory address register and the Exchange requests access to main memory. When the control word is received, it replaces the old control word in exchange memory.

A new control word is not obtained immediately because it would require the Exchange to dwell on the channel for an additional 1 microseconds. This would reduce the number of units that the Exchange could service simultaneously. By coming back to the channel after all other channels have been serviced, the Exchange makes use of what would otherwise be idle cycles. With the above arrangement, the Exchange never dwells longer than 2 microseconds at a time on a channel.

2.3.9 DISCONNECTING AN INPUT/OUTPUT UNIT

If the word count reaches zero and the control word does not contain a grouping/distribution flag bit, the unit is disconnected from the Exchange. The unit is disconnected by sending reset current down the channel assigned to the unit. This current turns off the crosspoint core at the intersection of the channel and the unit. The core going from the on to the off state generates a disconnect signal to the unit. An end of message signal is also sent to the Computer along with the address and status of the unit.

An end of message signal from an input-output unit can also cause the unit to be disconnected from the Exchange. If an end of message signal is received from a unit that is reading the information in the data word is shifted to the left end of the data word and transferred to main memory. The unit is then disconnected as described in the above paragraph. If an end of message signal is received from a unit that is writing, the unit is disconnected immediately as described in the above paragraph.

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2.4 LOW SPEED UNITS

2.41. GENERAL

Low speed units may be defined as those units which operate in the speed range of 0 - 100 bytes per second. Many units of this type may be handled simultaneously through a single channel in the Exchange. The maximum complement of low speed units has been set at 256 units.

Low speed units time share one channel on a byte by byte basis rather than being connected for an entire record as is the case with medium speed units. Each complete pass of the channel scanner will find a different unit connected to the low speed channel. The address of the unit is sent to the Exchange with each byte of information in order that the correct data and control words may be located.

There may be a wide variety of low speed units, which indicates there will be slight differences in the method of handling various types of units. The two large categories will be input units and output units. The input units can be further classified as to interrogation and non-interrogation types. Interrogation type input units are those that may request selection by the Computer. Non-interrogation type input units will deliver input information upon demand by the Computer.

2.4.2 LOW SPEED INPUT CHANNEL

The low speed input channel in the Exchange is made up of the following registers and control triggers.

a) Unit Address Register
b) Data Register
c) Ready Trigger
d) Select Request Trigger
e) Service Request Trigger
f) Control Word Modification Trigger
g) End of Message Trigger
h) Cancell Message Trigger

a) Unit Address Register - This register receives the unit address with each byte of data from low speed units. This address is used to locate the proper data word and control word in Exchange memory as well as for selection purposes when the input unit requests selection.

b) Data Register - The data register receives a byte of data from the input unit and holds it until it can be accepted by the input byte register in the Exchange.

c) Ready Trigger - The ready trigger receives the ready signal from the input unit and feeds this condition to the Exchange for storage as part of the status of the unit.

d) Select Request Trigger - The select request trigger is used by interrogation type input units. The unit requests selection by sending a signal which turns on the select request trigger. The output of the select request trigger, as well as the unit address, is sent to the Delta computer where selection takes place under program control.

e) Service Request Trigger - The service request trigger is turned on by a signal from the input unit to indicate that a byte of information is available in the input data register.

f) Control Word Modification Trigger - The control word modification trigger is turned on by the Exchange when the data word for a particular unit is fully loaded. It indicates that a control word modification cycle should be taken in order to get the data word address for storage of the completed data word in main memory.

g) End of Message Trigger - The end of message trigger is turned on by the input unit at the end of the record. The Exchange uses this indication to deselect the unit and indicate to the Delta computer that the record is complete.

h) Cancell Message Trigger - This trigger receives a cancell signal from an inquiry unit when the operator desires to cancell a record instead of letting it be processed by the computer.

2.4.3 LOW SPEED OUTPUT CHANNEL

The low speed output channel in the Exchange is made up of the following registers and control triggers.

a) Unit Address Register
b) Data Register
c) Ready Trigger
d) Service Request Trigger
e) Control Word Modification Trigger
f) End of Message Trigger
g) Prepare for Control Trigger

a) Unit Address Register - The unit address register receives the address of the particular low speed output unit currently connected to the channel. This address is used to locate the proper data and control words for servicing the particular unit.

b) Data Register - The data register accepts bytes of information from the Exchange to pass along to the output unit currently connected to the channel.

c) Ready Trigger - The ready trigger for output units serves the same function as for input units. It receives the ready signal from the output unit and sends this condition to the Exchange for storage as part of the status of the unit.

d) Service Request Trigger - The service request trigger is turned on by a signal from the output unit. It indicates that the output unit is ready for the next byte if it is in operation. When not selected, the low speed output units always send service requests which are ignored until the unit is selected.

e) Control Word Mod. Trigger - The control word mod. trigger is turned on by the Exchange to indicate that the data word for the unit on the channel has been completed. A new data word must be obtained from main memory, therefore, a control word cycle must be taken to get the proper main memory address.

f) End of Message Trigger - The end of message trigger is turned on by the unit. The Exchange uses this indication to deselect the unit and indicate to the Delta Computer that the record is complete.

g) Prepare for Control - This trigger is turned on by the Computer when control data is sent to the unit. The on condition of this trigger signals the unit to interpret the data as a control instruction.

2.4.4 SELECTION OF LOW SPEED UNITS

All selection of units is done under program control. However, interrogation type input units may request selection. To accomplish selection of any low speed unit, a select bit is inserted in the data word associated with the particular unit.

Interrogation type input units signal the Computer, under operator control, when selection is desired. This signal turns on the select request trigger in the low speed input channel at the Exchange when the particular unit is connected to the channel. The Exchange sends the select request and unit address to the Delta computer where selection is made under program control. The input unit is locked out until selection is completed. Reject signals are sent to the unit each time it appears on the channel until the select for Read flag bit is present in its data word. When the Computer finally selects the unit, a response signal is sent to the unit the next time it is connected to the channel. This response unlocks the unit and allows the input data to be entered at will.

Whether selected or not, all low speed units send service request signals. These service request signals cause the Exchange to obtain the data word associated with the unit. If the data word contains a select flag bit, the unit is serviced in the normal way and a response signal is sent by the Exchange. If the data word does not contain a select bit, the service request is ignored and the Exchange sends a reject signal. Once a unit is selected, it sends service requests only when service is needed. Disconnect occurs when the word count reaches zero or when the unit sends an end of message signal. End of message will be sent to the Delta computer in order that the program may be informed when a record is complete and ready for processing.

2.4.5 READING AND WRITING WITH LOW SPEED UNITS

Within the Exchange, reading or writing with low speed units proceeds in the same way as with medium speed units.

2.4.6 OPERATOR CONTROLLED MESSAGE REJECTION

If the operator makes an error in sending information from an inquiry station, the entire message may be cancelled by the operator. If a keying error is realized by the operator during a message, the cancell key may be depressed. This key sends a cancell signal to the input channel. The Exchange uses the cancel signal to remove the select bit from the data word and the unit is effectively disconnected. Since no end of message signal was received by the Computer, no action will be taken on the partial record. If the operator desires to send the message again, a select request must be made first and the record can be started again.

2.4.7 ERROR DETECTION

All information traveling between the Exchange and input-output units will contain a parity check. Any single bit transmission error will be recognized and indicated. Error correction will depend on the program or operator for proper action in the case of low speed units.

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2.5 HIGH SPEED OPERATION

2.5.1 GENERAL

In order to provide information handling facility for the X10 magnetic tape, several channels can be provided through which information flow is on a word rather than a byte basis.

2.5.2 WORD CROSSPOINT SWITCH

To provide the above facility, a word crosspoint switch is used which is similar to the byte crosspoint switch described previously, except that it can switch 72 bits in parallel rather than 9. Eight X10 tape units can be permanently connected to the system. Four can be operated simultaneously, either reading or writing. This is in addition to the simuntaneous operation provided by the Basic Exchange.

2.5.3 WORD CHANNEL SERVICING

The 4 channels are scanned by the same channel scanner used for the byte crosspoint switch. Operation is identical to the byte crosspoint switch with the exception that the words are not routed through the Exchange memory but instead are transferred directly between the main memory and the word crosspoint switch.

Each time a service request is received on one of the 4 full word channels, a data word transfer cycle is taken wherein the word is transferred from the crosspoint switch to the location in main memory specified by the data word address in the control word if reading; or if writing, a word is transferred from the main memory location specified by the data word address in the control word to the proper intersection in the crosspoint switch.

The data word accumulation feature of the Exchange is not necessary since full words are transferred parallel by the bit. However, the control of the units attached to the word crosspoint switch by the Exchange is otherwise identical to those connected to the byte crosspoint.

2.5.4 ECC BITS

The 72 bit words transferred via the word crosspoint switch include ECC bit. The word will be checked within the input-output unit and at a check station between the Exchange and main memory.

2.6 CHECKING FACILITIES OF THE EXCHANGE

Checking stations are incorporated to provide the features of error detection and correction, to facilitate unattended operation and to allow isolation of the error to a specific location. Minimum checking is provided for inputs to the system from external sources not using error correcting codes. Maximum checking occurs for information generated within the system, where the error correcting code is recorded with the data.

The Exchange directly transfers to the Delta Computer words which contain the error correcting code (ECC). The ECC for single error correction consists of 8 bits added to the 64 bit word. Seven of these parity bits provide the feature of single error correction. By adding an overall parity bit, double-error detection can be realized. They are incorporated to provide the Delta Computer with the flexibility of being able to perform single error correction and double error detection on information at arbitrary points in the system.

2.6.1 CHECKING BETWEEN THE EXCHANGE AND THE COMPUTER

Seventy-two bit words, 64 data bits and 8 ECC bits, are transferred between the Exchange and the main memory. There are either data words or control words for the I/O units.

At the discretion of the programmer, the Exchange can operate in either one of two basic modes. The checking facilities provided for information which circulates within the system are more extensive than for information used in conjunction with external systems not using the ECC. Recording of the ECC on all I/O devices used exclusively within the system is required, whereas it is assumed that the information which intercommunicates with other systems may contain no error correcting code. The two modes of operation with respect to checking are as follows:

Mode I.

When the information being communicated between the Exchange and the I/O devices does not contain within itself, the ECC, the Exchange accumulates or disassembles a 64 bit data word. When reading, as the data word is transferred to the Computer, the Exchange generates 8 bits of ECC along with the 64 bits of information to be routed to the main memory. In an output operation, the Exchange sends only the 64 bits of information to the output unit. The 8 bits of ECC are discarded.

Mode II.

This mode of operation allows complete error correction and detection. When the information being communicated between the Exchange and the I/O devices does contain within itself the ECC, the Exchange accumulates up to 72 bits of information from the unit before it is transferred to the main memory. The last 8 bits of information are the ECC bits.

On output operation, the entire 72 bits of information, which includes the ECC, are sent to the output unit. The ECC bits are recorded on the output media and are read back as part of the word.

An ECC checking station is located on the buss lines between the Exchange and the main memory. It is possible, with the proposed code system, to detect double errors or multiple even errors and to specify the location and thus to correct any single error. However, it is not possible to determine whether an error is multiple or single when the number of errors is odd. The ECC checking station serves to check the validity of the information that communicates between the Exchange and the main memory as follows:

a) It executes single error correction and double error detection on all the control words and the data words as they are being shipped from the main memory to the Exchange input register.

b) When operated in Mode II, the data word is verified before it is transferred to the main memory. The Mode I operation calls for the generation of 8 bits of ECC which along with the information, are routed to the main memory. The generation of the ECC makes use of the same circuit as that used for checking and correcting.

The errors will be indicated and recorded to facilitate maintenance. The recorded information consists of:

1) The word in error
2) The type of error
3) The bit position in error for single error
4) The I/O unit address
5) The input channel, and
6) The time of error.

2.6.2 CHECKING WITHIN THE EXCHANGE

The Exchange is designed to be able to accept or distribute information either on a character basis or on a word basis. Byte-wise, the communication between the Exchange and the character type I/O devices consists of 9 bits. The ninth bit is an even-odd parity bit for the character. For those I/O units whose character size is not a multiple of 8, it is necessary to have peripheral equipment to convert the characters to a standard 8 bit byte plus a parity bit. The peripheral equipment preserves the continuity of the parity check.

Information circulated within the Exchange is checked only by the parity bit. Checking stations are located at three points.

1) Input Byte Register
2) Output Cross Point Switch
3) Word Register.

During input operation, either the byte carries a parity bit, which will be checked both at the input unit and after reading out of the input crosspoint, or the byte does not carry a parity, in which case, a new parity bit is generated prior to sending the byte to the Exchange. A byte of information is checked by a parity checker as it is transferred through the Input Byte Register to be accumulated. An error would be detected and recorded along with those indicated by the ECC checker each time a full word is transferred to the main memory. Transmission errors and errors from the input unit are differentiated by different error triggers attached to the channel. The byte parity bit is dropped before the byte of information is read into the Exchange memory.

During an output operation, a parity bit is generated for the character that is being transferred out of the Exchange memory. This byte of information, together with its parity bit are sent to the output crosspoint. No checking is provided at the Output Byte Register. A parity checker will be inserted to check the validity of the information read out from the output crosspoint. It serves to detect any transmission error or error introduced at the output crosspoint.

All information that communicates between the Exchange memory and the word register is checked with respect to an overall even-odd parity bit by a parity checker inserted at the word register. An error will be recorded whenever the checking fails. The recorded information includes the word in error, the Exchange type cycle, the time of the error and the I/O unit address which also specifies the address of the word in the Exchange memory.

The parity bit for the data word and the control word should be modified in accordance with the type of Exchange operations executed. The modification of the parity bit falls into three forms:

a) The byte count of the data word is stepped down by 1 during each data word subcycle.

b) The word count section of the control word is stepped down by 1 during each control word modification cycle.

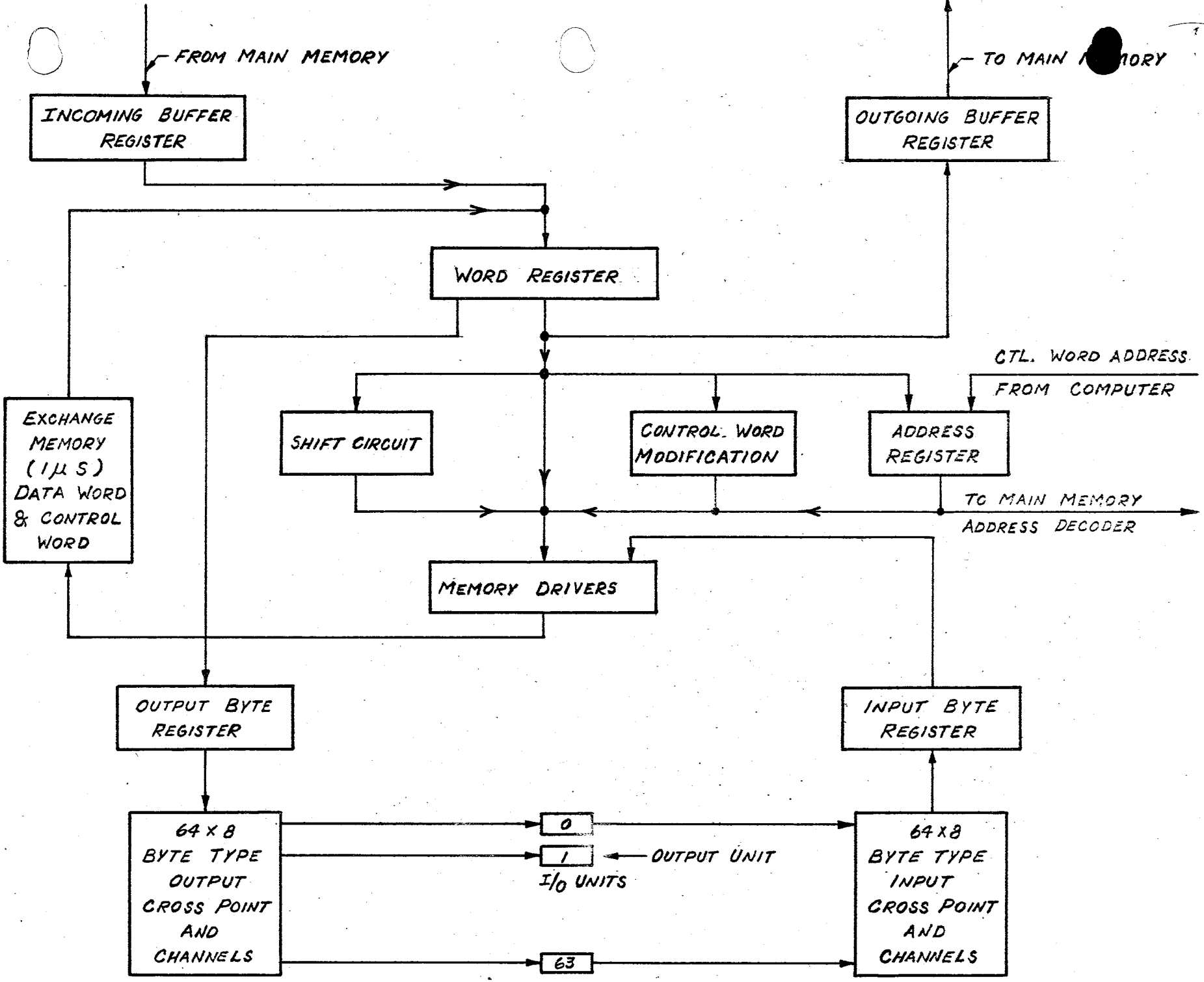
c) The data word address of the control word is stepped up by 1 during each control word modification cycle.

Eight bits of data are being added into the data word during an input data word subcycle. The partially filled data word with the present byte count are checked as they are read out of the Exchange memory into the word register. A new parity bit is generated by making use of the original parity, the parity of the added byte and the present byte count before it is stepped down by 1.

Eight bits of the data are being disassembled to the output register during an output data word subcycle. The parity bit for the partially disassembled data word is checked at the word register. A new parity bit for the remaining of the data word can also be generated by making use of the original parity, the parity of the byte being transferred, which is generated at the output register, and the present byte count before it is stepped down by 1.

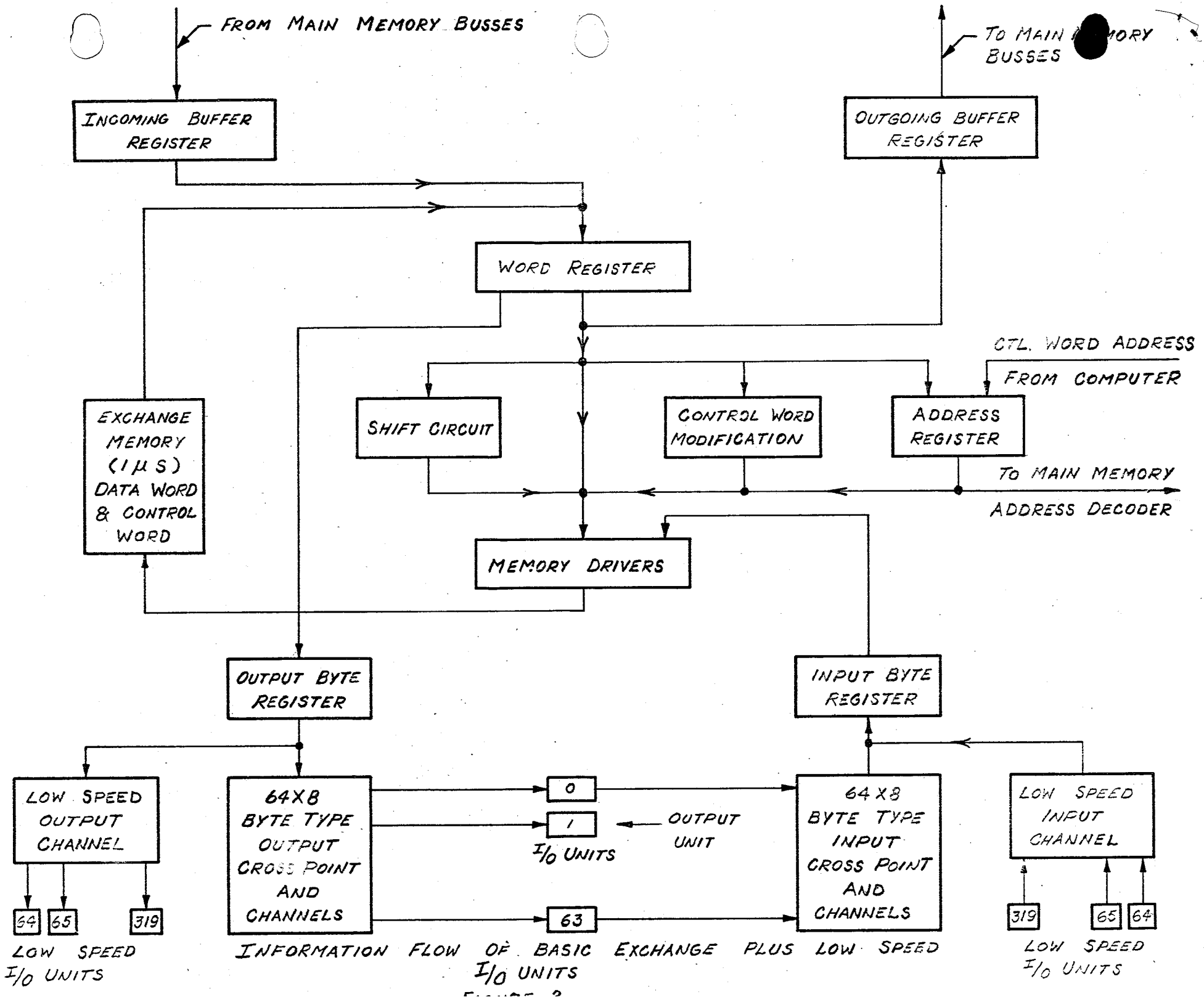
The parity bit associated with the control word is checked at the word register during a control word modification cycle. As the data word address and the word count are being modified, a parallel operation is carried out during which a parity for the modified control word is generated. It makes use of the original parity of the control word and those bits in the word count and the data word address before they are modified.

All detected errors will be recorded along with the time and the place of their occurrence. It will allow the maintenance group to pinpoint the location of the error to a specific logical area. When the system operates as a closed system, almost complete error detection and correction is available.



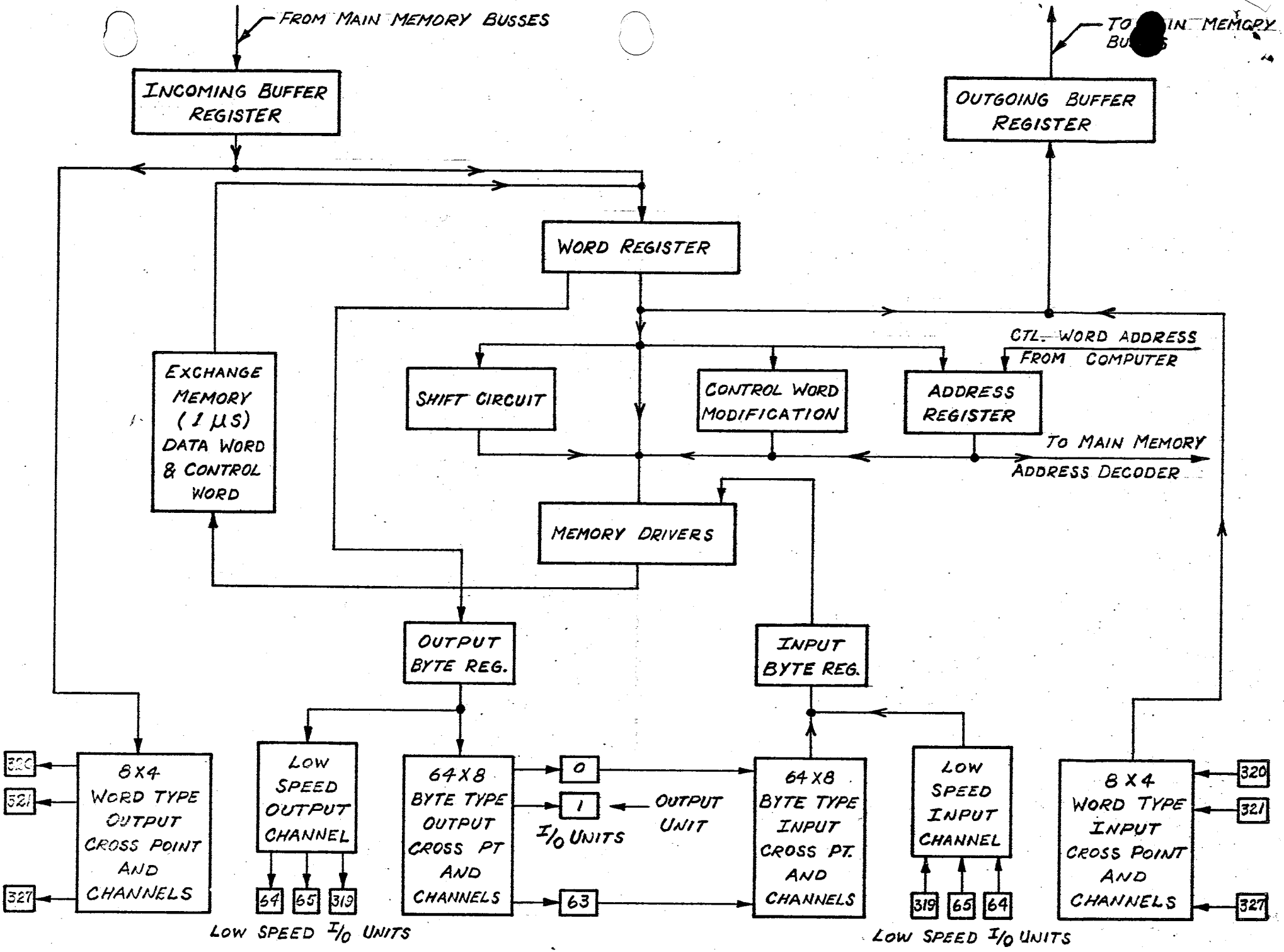
INFORMATION FLOW OF BASIC EXCHANGE

FIGURE 1



INFORMATION FLOW OF BASIC EXCHANGE PLUS LOW SPEED I/O UNITS

FIGURE 2



INFORMATION FLOW OF BASIC EXCHANGE, WORD OPERATION AND THE LOW SPEED I/O UNITS

FIGURE 3

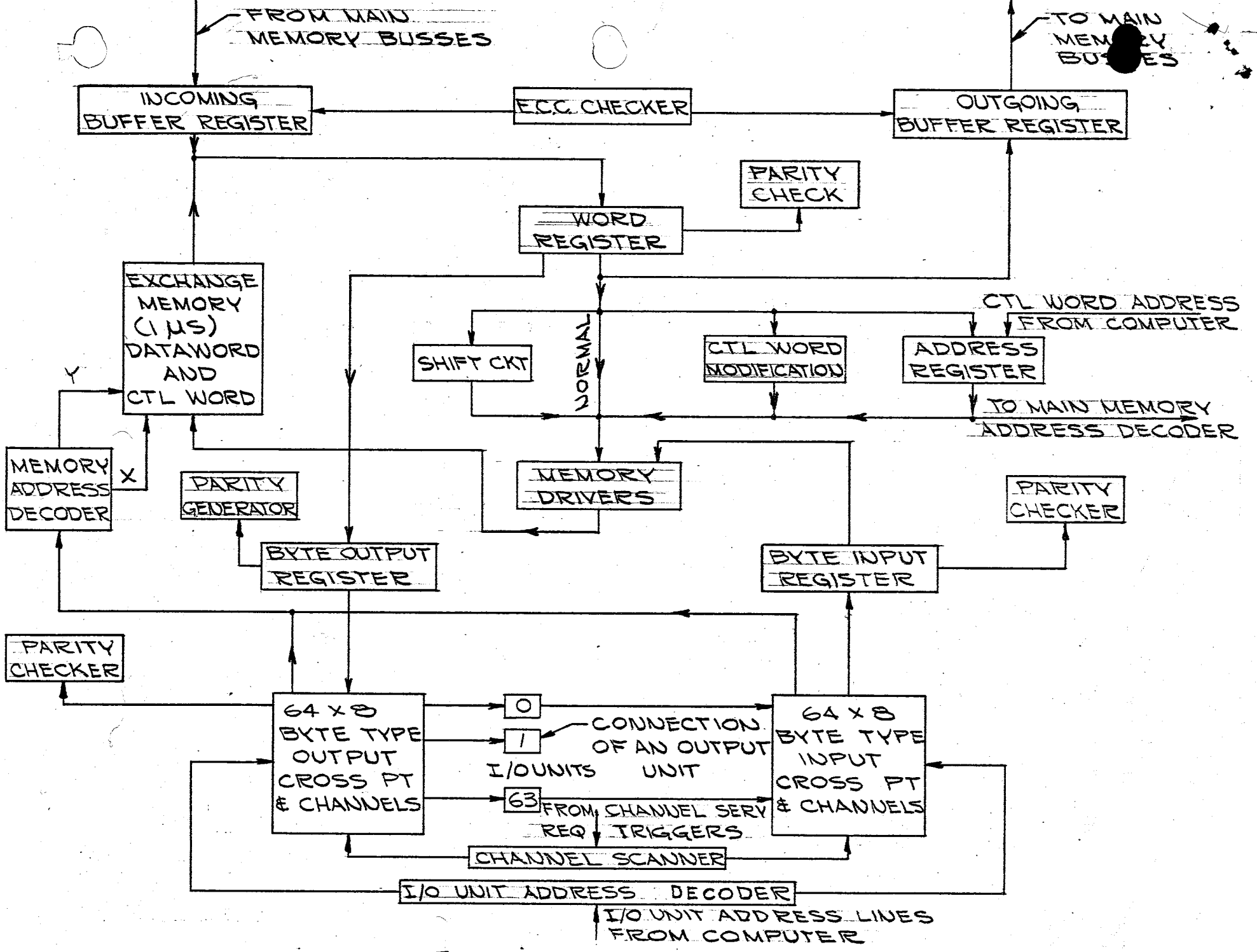


FIGURE 4
BASIC EXCHANGE WITH CHECKING