Project 7000

Maintenance Development Memo #12

SUBJECT: Marginal Inspection of Current Switching Mode Transistor Circuits

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Introduction

The objective of Marginal Inspection is to detect any circuit which has an appreciable probability of causing computer failure in normal operation before the next Marginal Inspection is performed. Marginal Inspection may be defined as a systematic variance of circuit parameters, such as voltage and/or frequency, to the point where circuits that contain components that are beyond end of life specifications, fail to operate satisfactory. The value of the variance, or excursion, which causes a circuit to malfunction is called the circuit margin. Marginal Inspection does not reduce the number of failures observed in a system, only groups these failures into a narrow discreet region of time, which is under control of the engineer maintaining the machine or system.

Conclusions

Marginal Inspection of current switching mode transistor circuits will be an entirely practical method of increasing the reliability of computing systems using these components. Reliability being defined as the probability of error-free operation for a specified period of time. Delay failure will be a common occurrence while Marginal Inspecting and rapid means of detecting this type of failure will have to be provided.

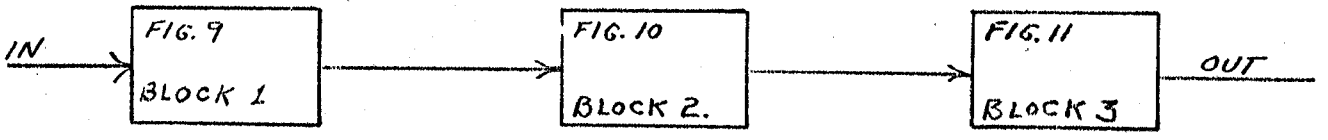
Part I Analysis of single blocks of current switching mode transistor logic under Marginal Inspection

Throughout this discussion, the higher collector return voltage will be considered the Marginal Inspection voltage. The values of these voltages being: Plus thirty and Minus thirty-six for "exclusive or" circuits, Minus twelve on "P" lines, and Plus six on "N" lines. Emitter source and base reference voltages will have to be independent of collector

return voltages so that we can vary one and only one voltage at a time. The voltage excursion necessary to produce switching failure on a variety of circuit configurations is shown on figures one through eight. The circuit configuration which shows switching failure with the least voltage variation is our prime concern as this circuit effectively sets the theoretical maximum margin of any system of which it is a part. Further study of the figures, one through eight, will indicate that the minimum percentage change to produce switching failure will be as follows:

Plus thirty, plus or minus 10%
Minus thirty-six, plus or minus 10%
Minus twelve, plus or minus 25%
Plus six, plus or minus 50%

Current mode transistor blocks will show some delay at normal voltage, with the larger values of delay being exhibited by heavily loaded blocks. The worst case delay value will probably fall in the range of twenty to thirty millimicroseconds on a block with full load, all components at end of purchase specifications, and one component at end of life. Results of Marginal Inspection voltage, applied to three logic blocks in series, is plotted in terms of delay on figures nine, ten, and eleven. Each figure is an individual plot of delay for the particular transistor block as noted:



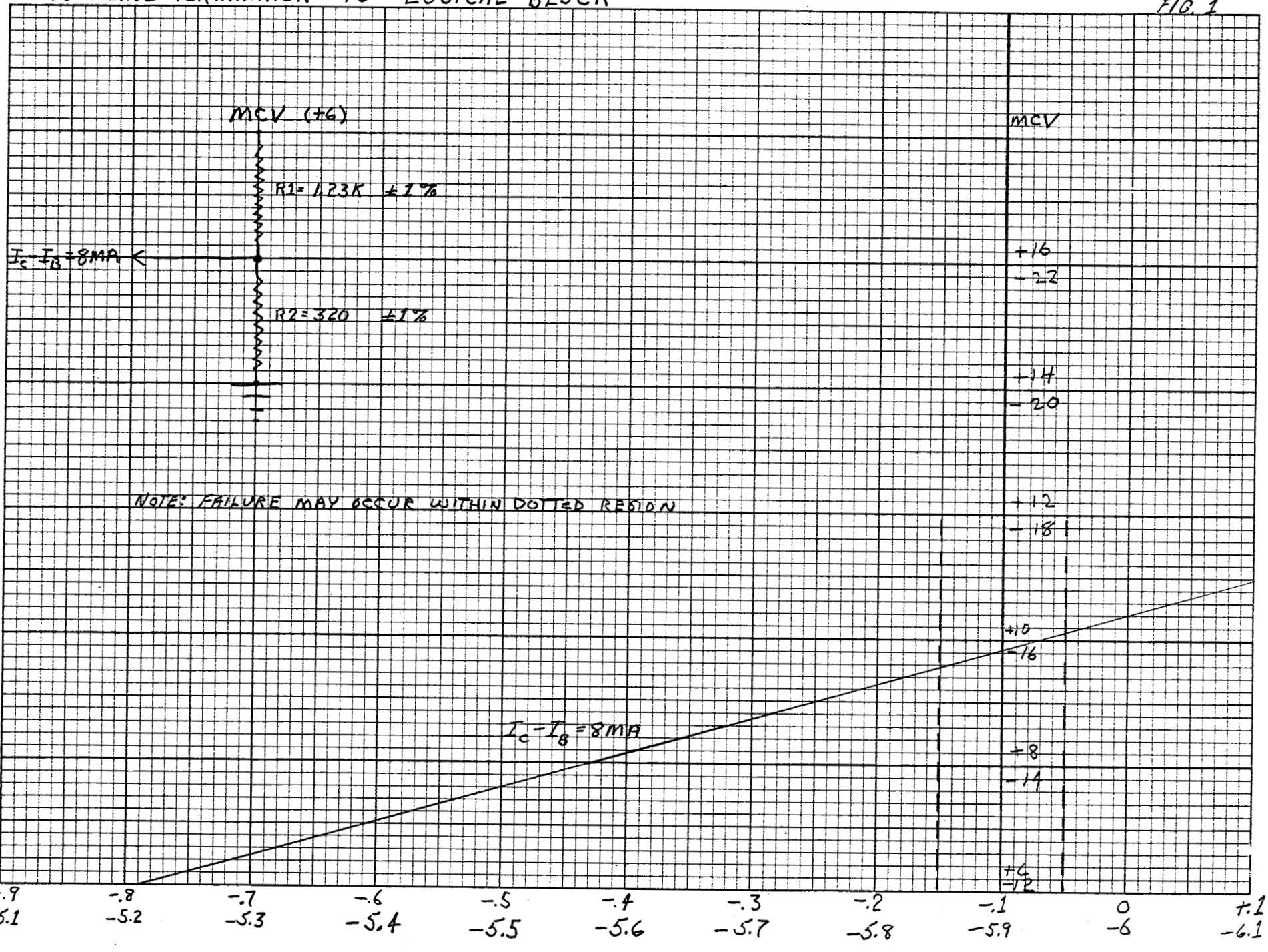
The curves on each figure represent the following conditions:

Curve 1. ---Normal block, one load
Curve 2. ---Marginal block, one load
Curve 3. ---Normal block, three loads
Curve 4. ---Marginal block, three loads

The termination of each curve is the point, in terms of Marginal Inspection voltage, where switching failure occurred. The effects of Marginal blocks was simulated by a change in emitter source voltage of twelve percent on plus six supplies and nine percent on minus

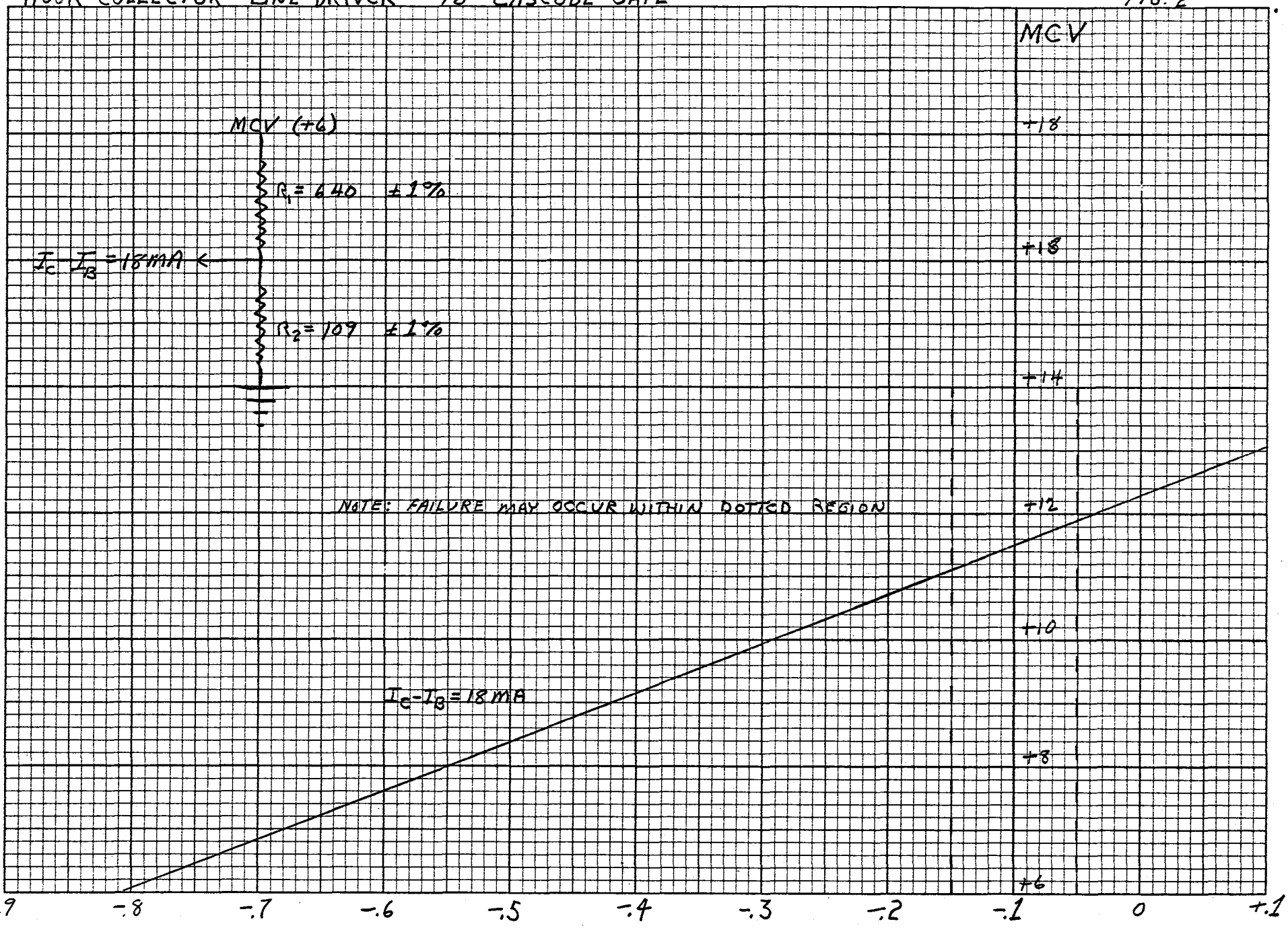
93Ω LINE TERMINATOR TO LOGICAL BLOCK

FIG. 1



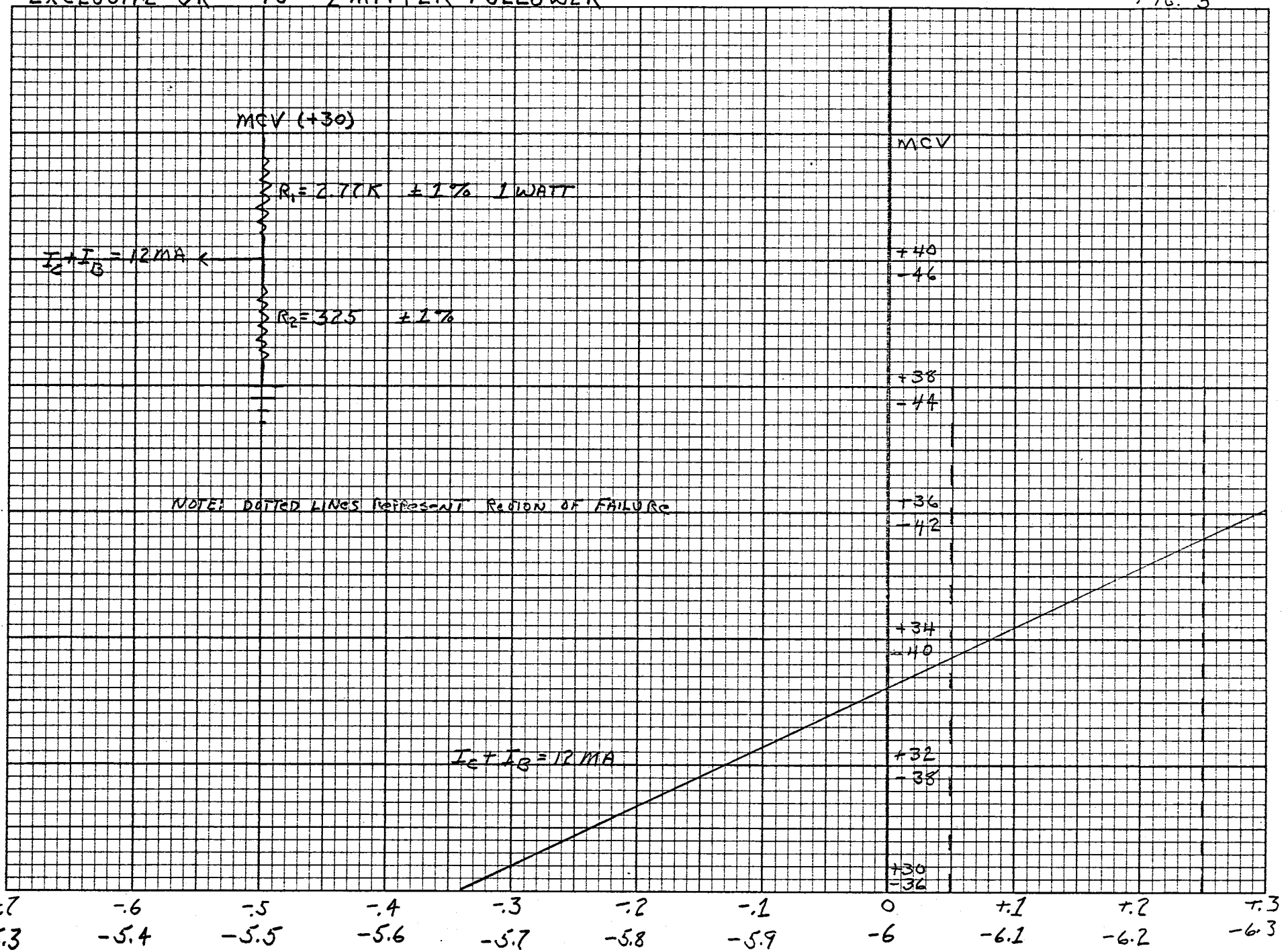
"HOOK COLLECTOR" LINE DRIVER TO CASCODE GATE

FIG. 2



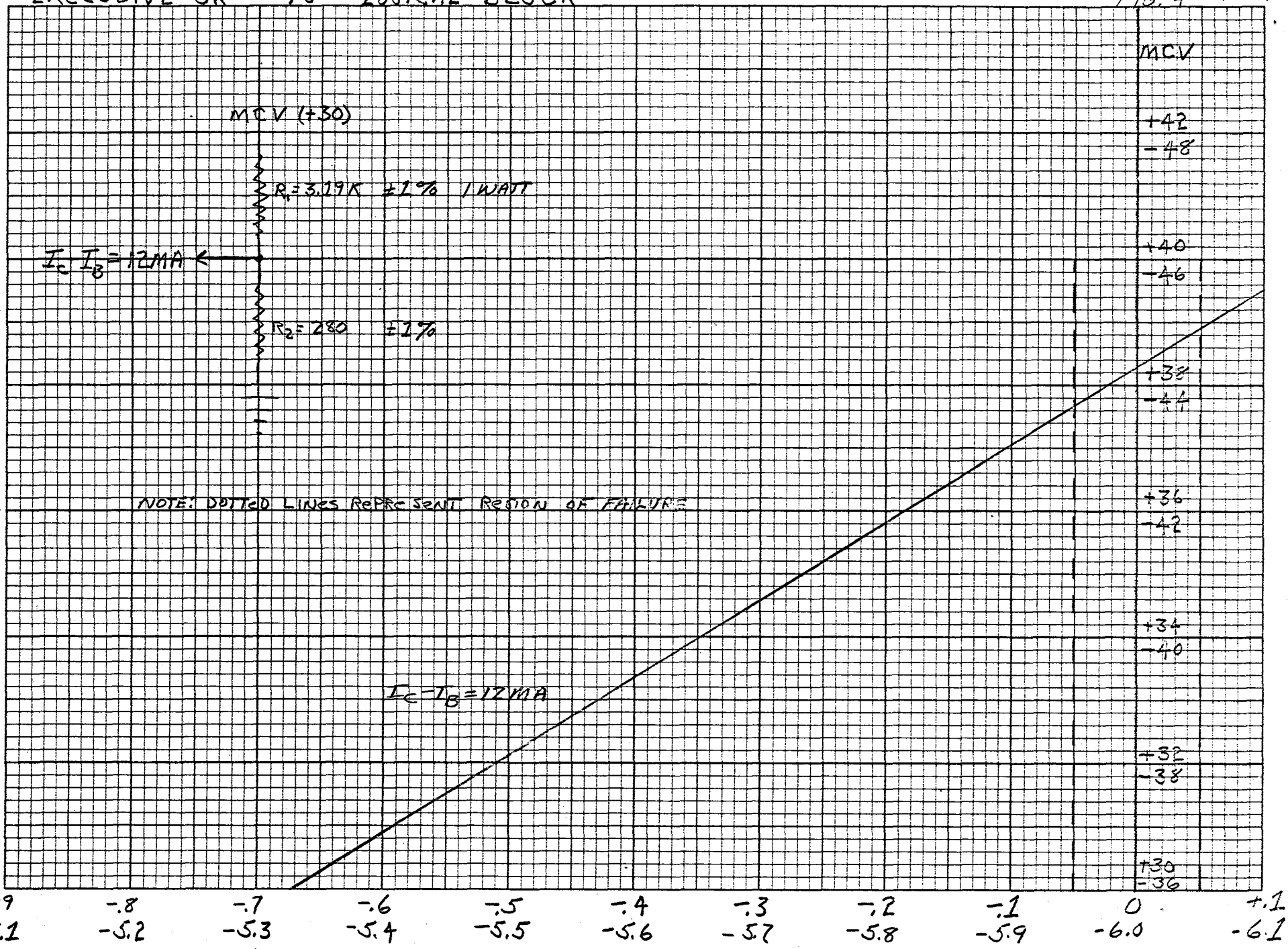
"EXCLUSIVE OR" TO EMITTER FOLLOWER

FIG. 3



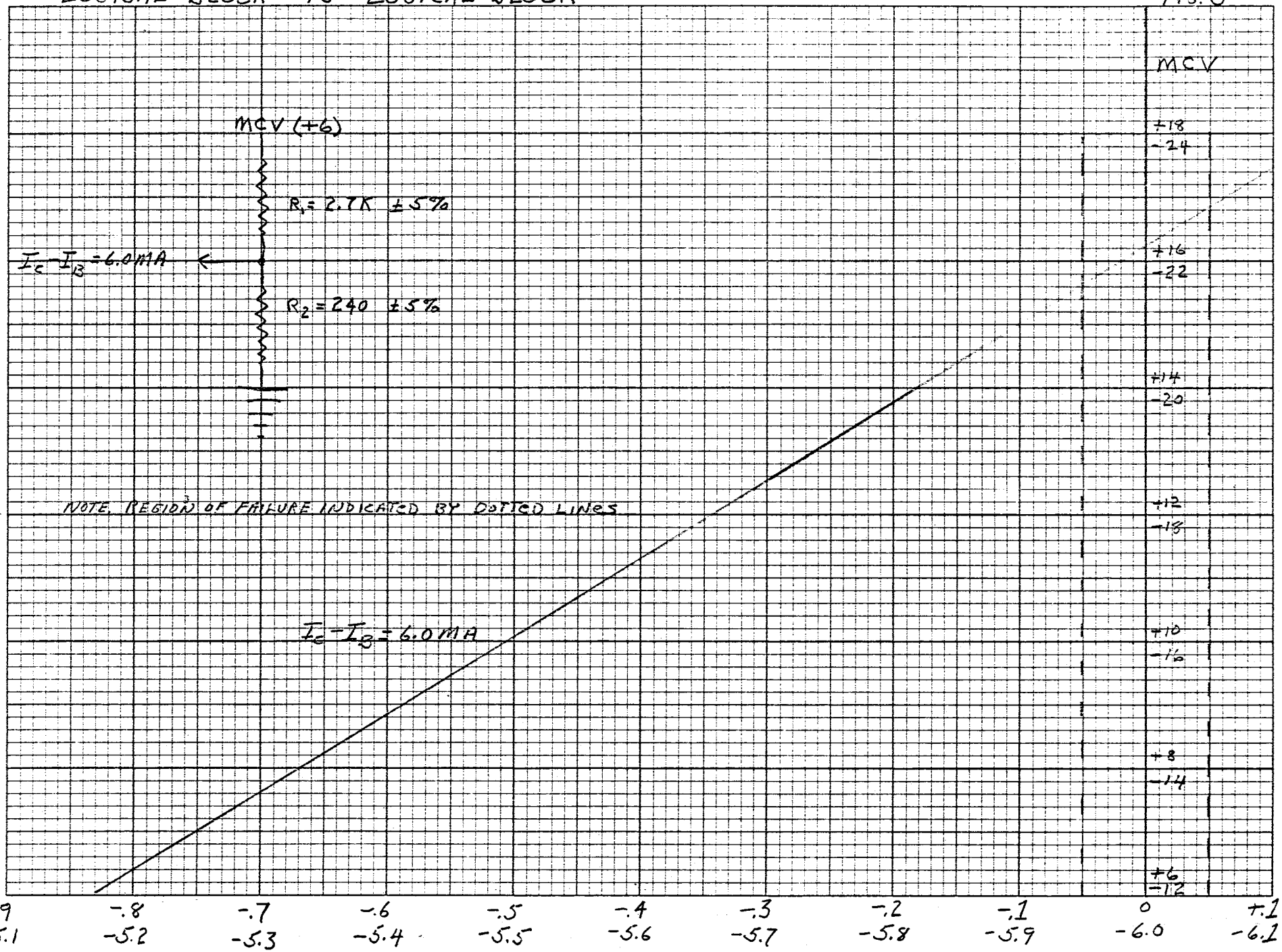
"EXCLUSIVE OR" TO LOGICAL BLOCK

FIG. 4



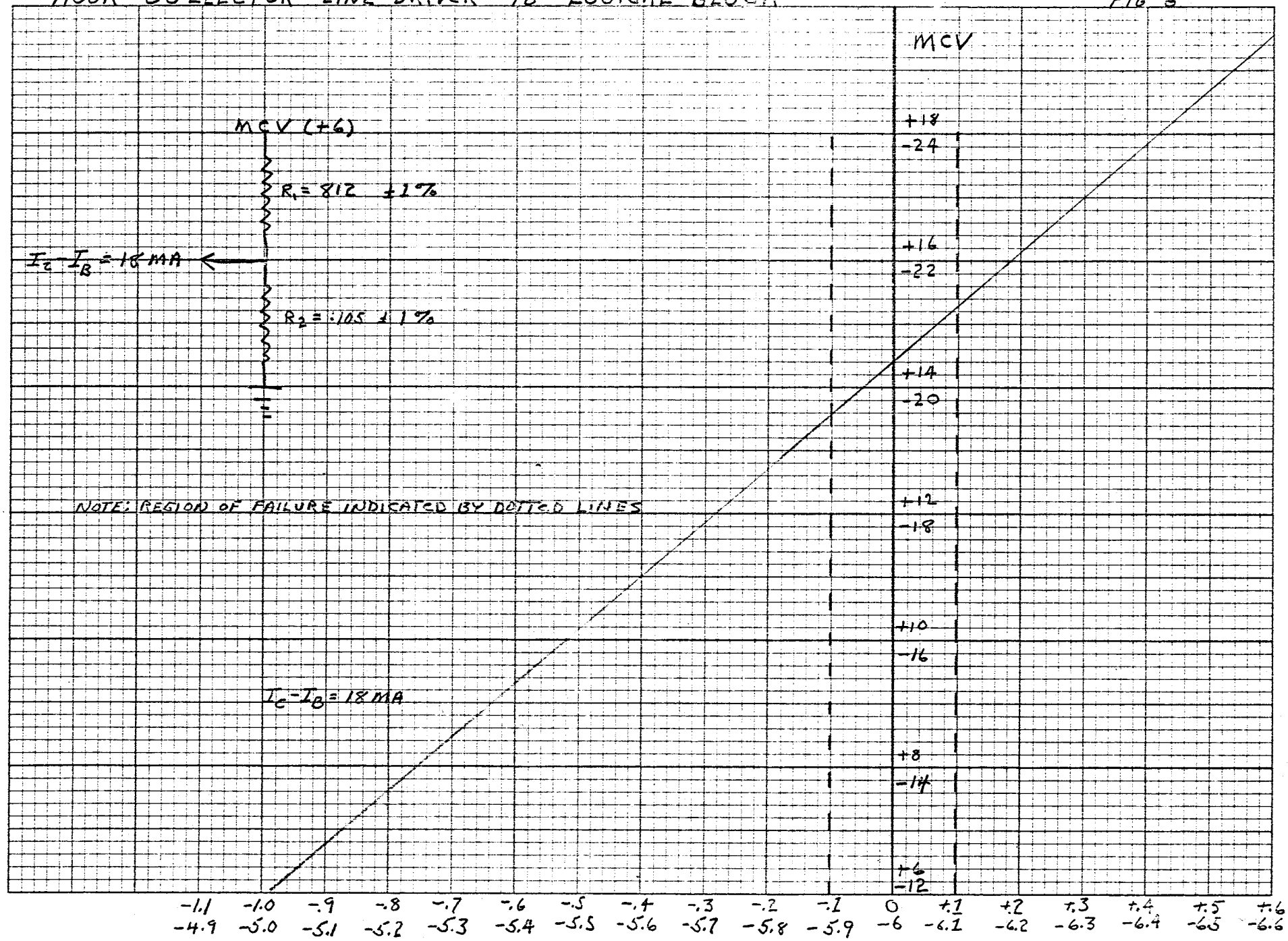
LOGICAL BLOCK To LOGICAL BLOCK

FIG. 5



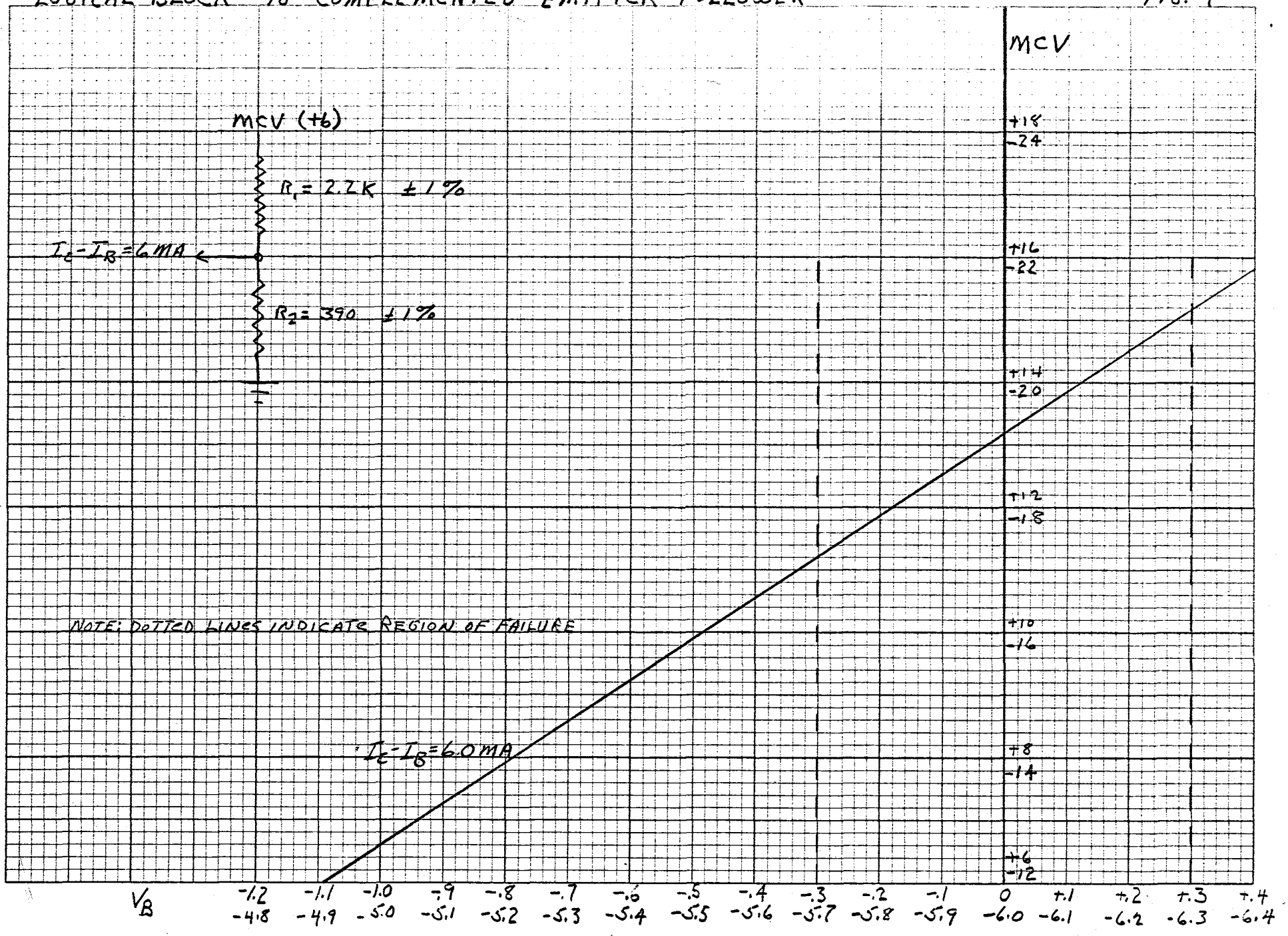
"HOOK COLLECTOR" LINE DRIVER TO LOGICAL BLOCK

FIG 6



LOGICAL BLOCK TO COMPLEMENTED EMITTER FOLLOWER

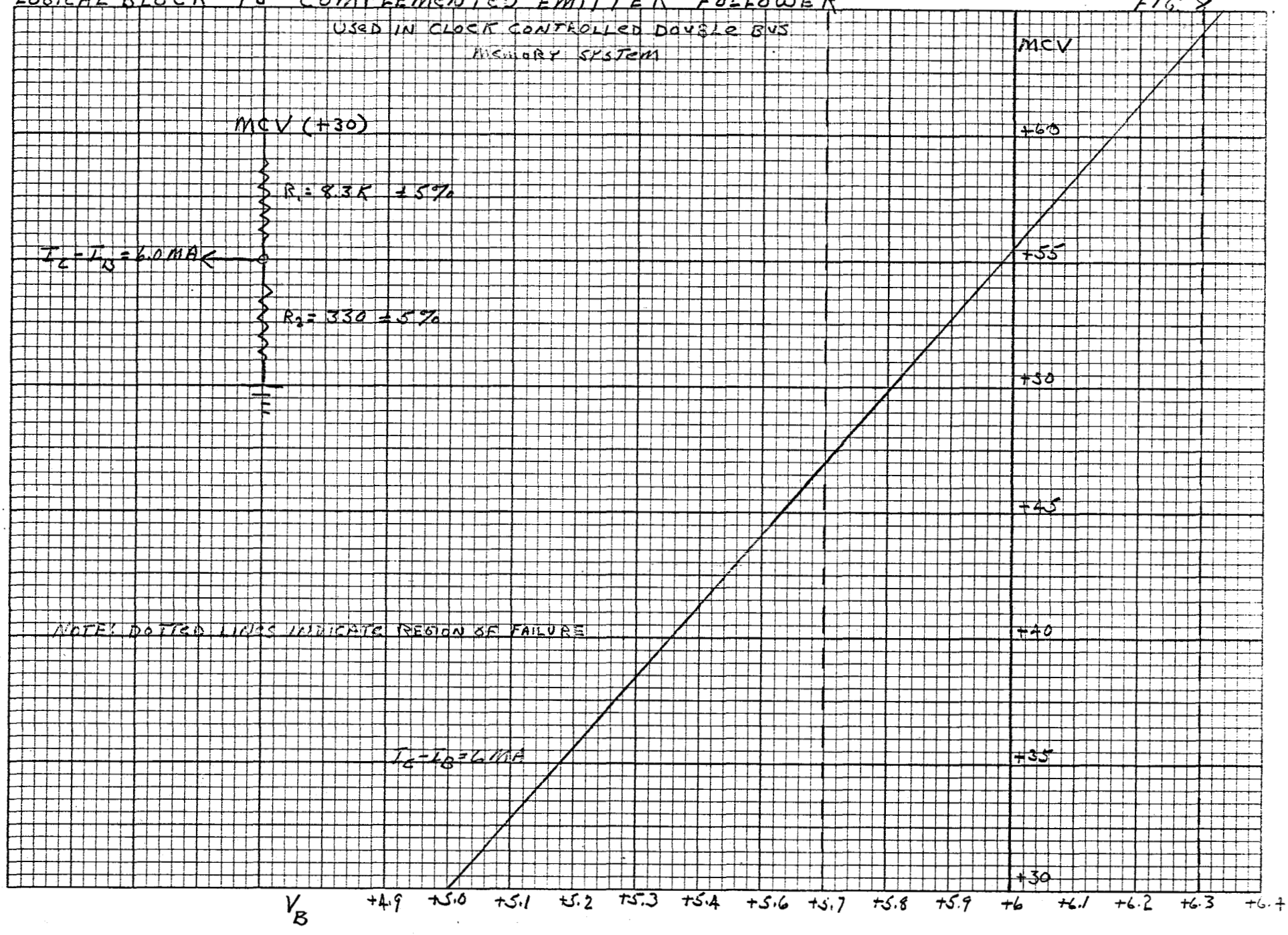
FIG. 7



LOGICAL BLOCK TO COMPLEMENTED EMITTER FOLLOWER

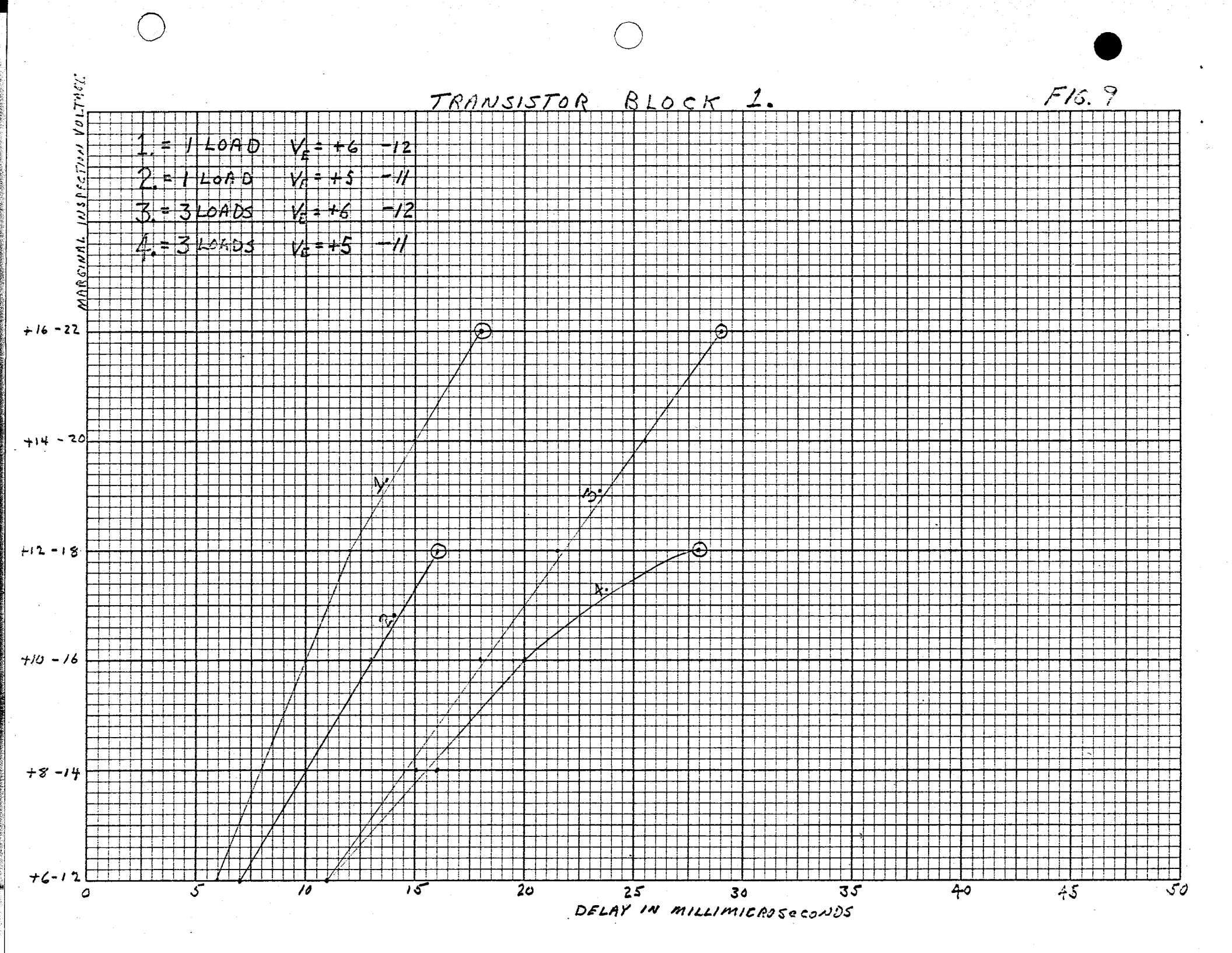
FIG 8

USED IN CLOCK CONTROLLED DOUBLE BUS MEMORY SYSTEM



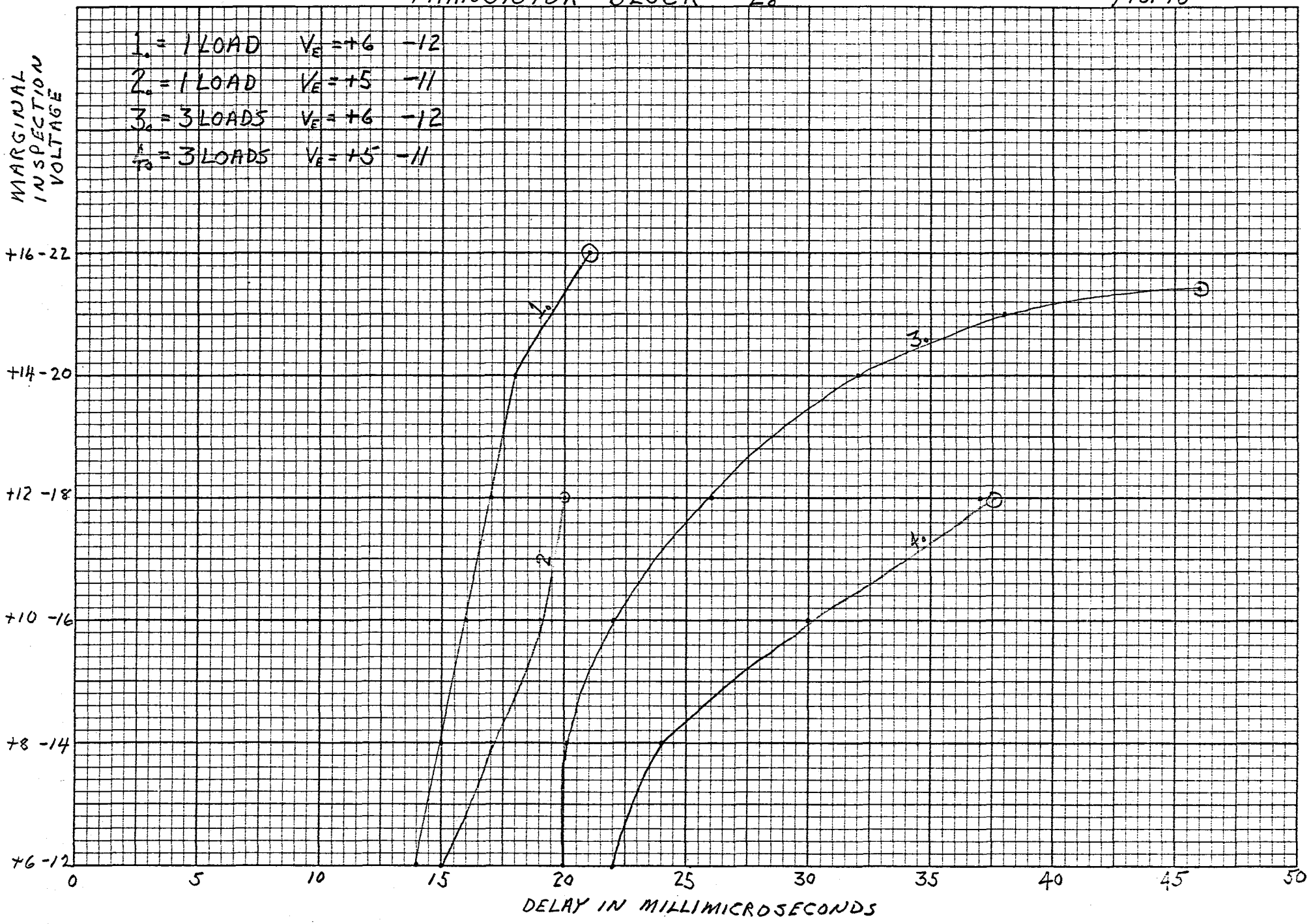
TRANSISTOR BLOCK 1.

FIG. 9



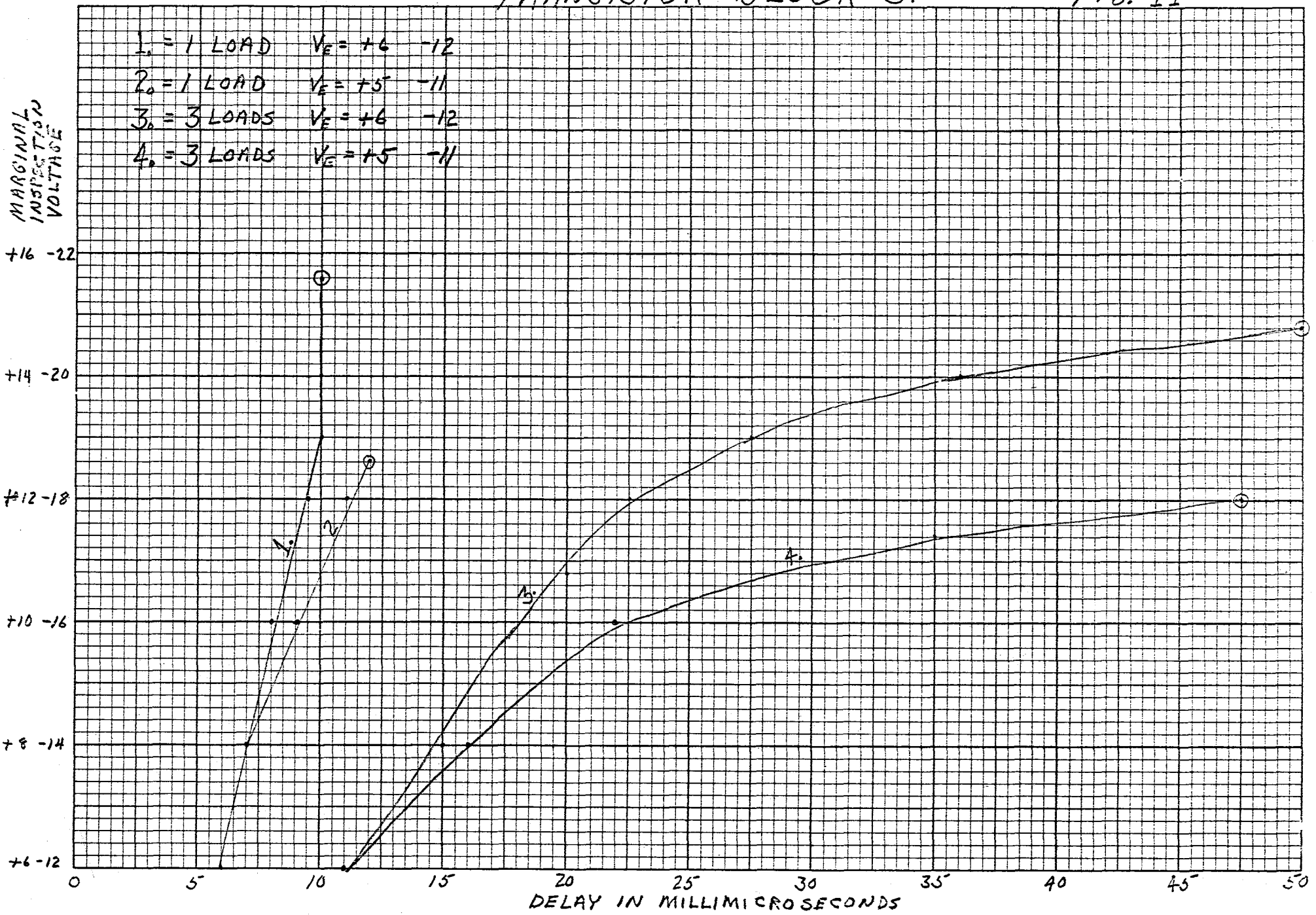
TRANSISTOR BLOCK 2₀

FIG. 10



TRANSISTOR BLOCK 3.

FIG. 11



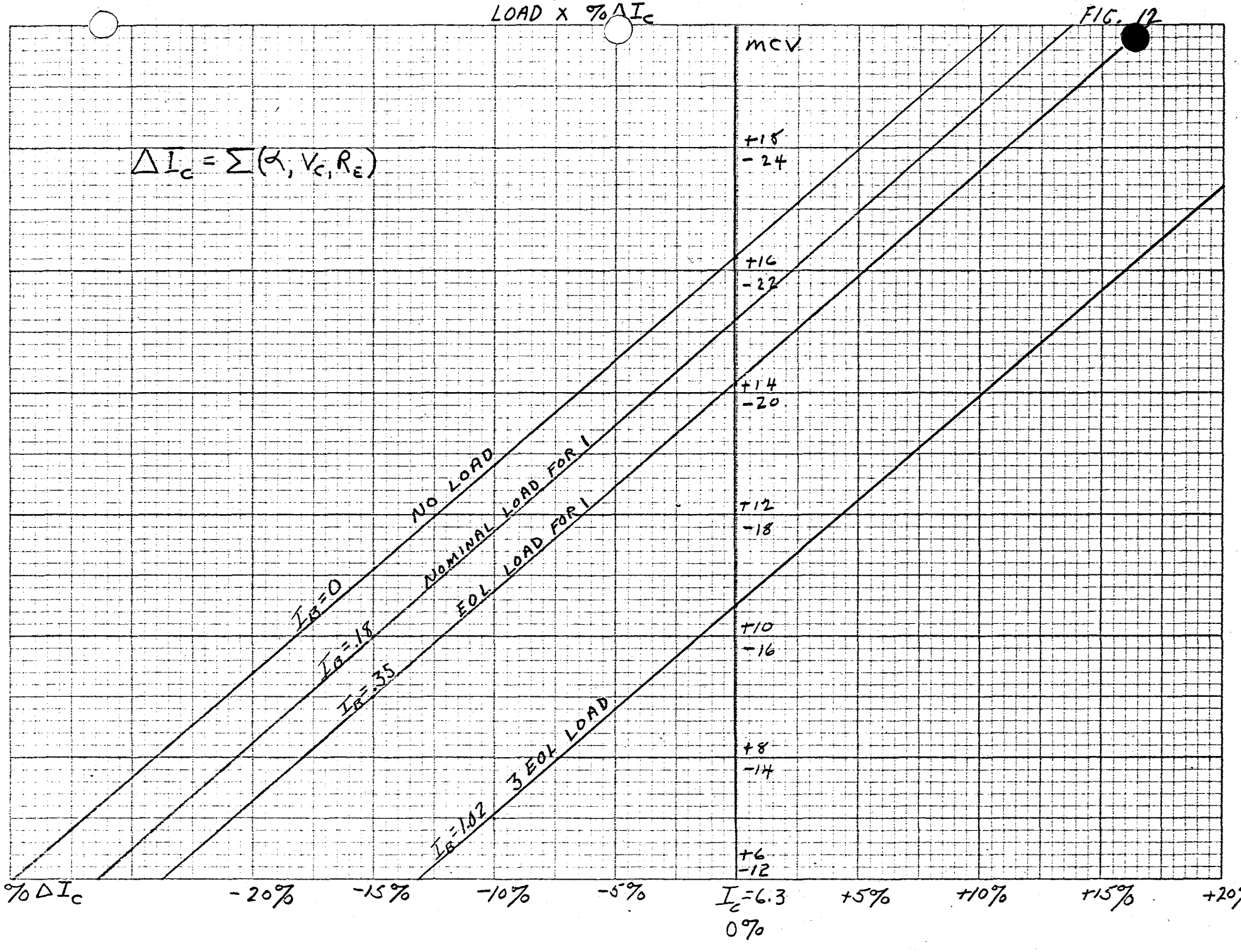
twelve supplies. We can see that normal blocks with one load exhibited small changes in delay as Marginal Inspection voltage was increased and blocks with three loads showed large increases in delay under the same conditions. It is to be noted that all these tests were performed with five percent components in the blocks. The switch to one percent components should not significantly effect the conclusions drawn here, with the exception that changes in value that were called limit of purchase specifications, now will be end of life. When investigating delay, we observed that loading had a definite effect on the operation of a block both at normal and under Marginal Inspection. We also observed that a change in I_C, as was simulated by a change in V_e, had a definite effect on the operation of a block. Figure twelve is a plot of Marginal Inspection voltage against percent change in I_C. The only conclusion that can be drawn from this plot, is large changes in I_C will be required to significantly change the switching failure point.

While investigating the behavior of single blocks of transistor logic under Marginal Inspection, no attempt was made to analyze frequency response. It was felt that a nominal variation of input frequency would have little affect on the operation of a single block and would only exert an influence on complete systems of logic, which will be treated in more detail under the systems portion of this discussion.

Part II Analysis of effects of Marginal Inspection on complete systems of logic.

Part I of this discussion dealt with the most obvious effects of Marginal Inspection on single blocks of transistor logic. We know that circuits in a computer are not isolated, they exist in combinations with other circuits to form large complex systems. In the absence of a large scale ten megapulse computer to try Marginal Inspection on, we must use a hypothetical system and extrapolate our results from single block analysis into system analysis.

Following the general form of the "Basic" computer of Project 7000, our hypothetical machine will be synchronous, use fixed delays, and operate at ten megapulses. The computing system under consideration consists of five logical stages operating in a serial fashion. Each logical stage consisting of no more than ten levels of transistor logic. We will handle eight bits of information in parallel and latch this information at the end of each logical stage. The information is passed from the latch circuit of one logical stage into the next stage by clock pulses having a repetition rate of two hundred millimicroseconds. For this discussion


LOAD x %ΔIc
FIG. 12
mcv
ΔIc = Σ(α, Vc, RE)
+18
-24
+16
-22
+14
-20
+12
-18
+10
-16
+8
-14
+6
-12
NO LOAD
NOMINAL LOAD FOR 1
EOL LOAD FOR 1
3 EOL LOAD
IB=0
IB=.18
IB=.35
IB=1.02
%ΔIc
-20%
-15%
-10%
-5%
Ic=6.3
0%
+5%
+10%
+15%
+20%

we will assume enough error detection circuitry is included so we can detect any single error that occurs in data transfer.

The Marginal Inspection voltages for this system will be the higher collector return voltage, plus thirty, minus thirty-six for "exclusive or" blocks, minus twelve on "P" lines and plus six on "N" lines. One and only one voltage will be varied at any one time. In the design of this hypothetical system, we will assume twenty millimicroseconds as the worst case delay for any transistor block.

Taking any logic chain of ten blocks and assuming all ten are at worst case delay, we can see by referring to figures 9, 10, and 11 that any increase in Marginal Inspection voltage will increase the delay through the chain to the point where failure occurs due to lack of coincidence with the clock pulse. While this is a serious problem, all is not lost, since all ten blocks at worst case delay at normal voltage means all ten blocks are at, or near, end of life. The more practical case will be for nine of the ten blocks to show nominal delay while the tenth is at worst case. Under these conditions, a much larger change in Marginal Inspection voltage is required to produce failure. The failure observed at this time may be a delay failure, but is much more likely to be a switching failure. To show why the above statement is true, we must look at a logic chain in more detail. Considering our chain of ten blocks and assuming we have designed for coincidence, at the output, with worst case delay through each block, we will be expecting two hundred millimicroseconds delay at normal voltage. But, we have already said that we were assuming only one block at worst case, therefore our delay at normal voltage is somewhat less than two hundred millimicroseconds actually being closer to one hundred millimicroseconds. Now as the Marginal Inspection voltage is increased the delay through each block increases, with the increase per block depending on loading and the condition of the block. Looking at figure 9, curves 1 and 2, we see that before worst case delay is reached on any block the marginal block has failed to switch. What we have actually done is let the safety factor in delay of the nine nominal blocks absorb the excess delay introduced by the tenth block. A general statement which encompasses this principal is as follows:

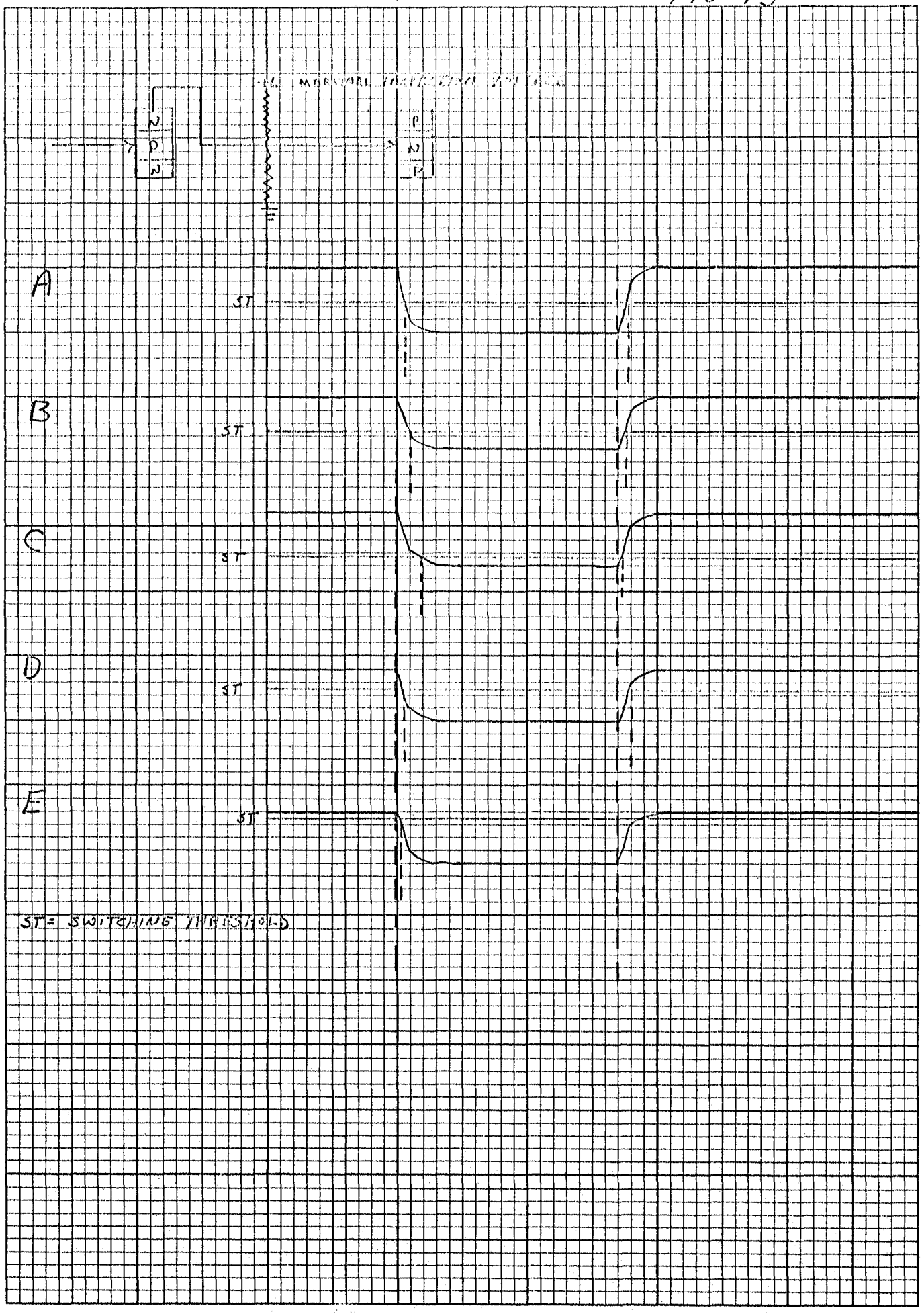
As the number of stages increases per logic chain, using the same criteria of design for worst case delay, the less susceptible to failure the string becomes due to excessive delay in a single block. When a

large string of logic blocks is Marginal Inspected we are really testing the summation of delays in the string and any variations in delay of a single block will be obscured. Therefore, while Marginal Inspecting a system, marginal blocks within long strings of logic will tend to show switching failure, while marginal blocks in short strings of logic will tend to show delay failure.

It is well to reiterate at this time, that we have been discussing a hypothetical synchronous type system. A true asynchronous type system would never show a delay failure. The only evidence of excessive delay being an increase in program run time as measured with a stopwatch, or analogue timers on the circuits themselves.

While discussing voltage variations needed to produce switching failure in a block of transistor logic, we pointed out that the higher collector voltage would have to be varied both plus and minus from its nominal value. Figure thirteen is an effort to show why this is necessary for Marginal Inspection. Waveform A is a representative signal applied to the base of a normal block. Low I_c in the "P" block, of this drawing, will result in a condition shown by Waveform B. What we have done is reduce the lower level of the signal so as to approach switching threshold. The increase in delay is indicated by the dotted lines on Waveform B. An increase in the Marginal Inspection voltage will shift the entire signal up as shown by Waveform C, increasing the delay through the block and bringing the lower level closer to the switching threshold. Thus, we have caused this marginal block to fail due to increased delay in time sensitive circuits and a small increase in Marginal Inspection voltage will cause switching failure in non time sensitive circuits. Taking the case of high I_{co} in the transistor block, we would get a waveform represented by drawing D. We can see that in this case an increase in the Marginal check voltage would have exactly the same effect as on a normal block. To detect this condition in a system will require us to lower the value of Marginal Inspection voltage, so as to approach switching failure from the opposite direction. A representative waveform of this condition with Marginal Inspection voltage applied is shown by Waveform E. We see that we are approaching switching failure and that delay, as indicated by the dotted lines, is increasing. The one important difference is that in this case the delay increase is not at the left side of the waveform but at the right, or it can be said we have turn off delay instead of turn on delay. This turn off delay will be as serious as turn on delay when considering machine failures. Where the turn on delay, if execssive, will eventually result in lack of coincidence at some gate circuit, the turn off delay, if excessive, will result in pluse overlaps at gate circuits, with resulting extraneous pulses.

FIG 13



ST = SWITCHING THRESHOLD

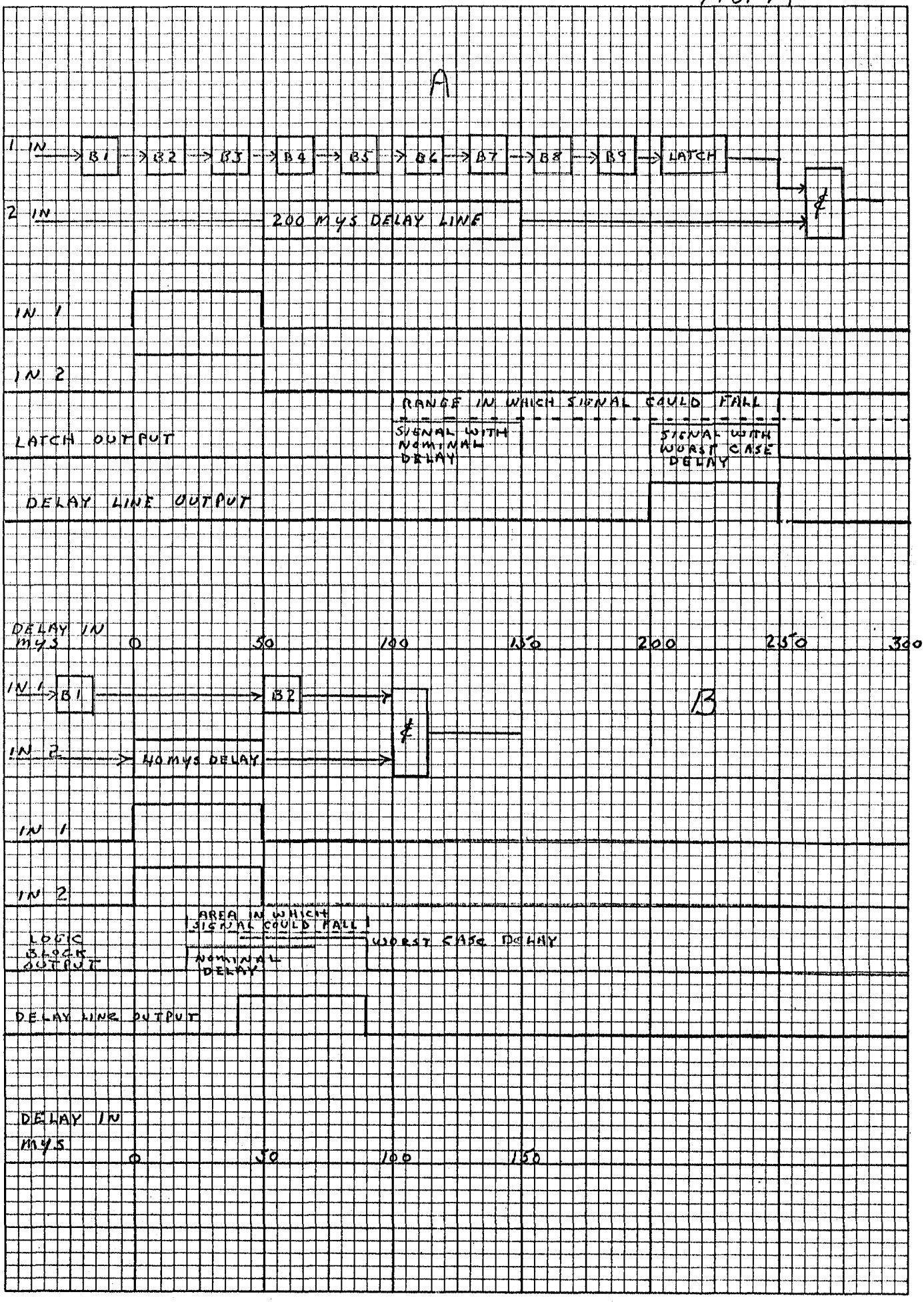
Fixed delays, such as single shots, delay lines, memory cores and I/O devices require some special attention in these delay sensitive systems. Single shots and delay lines may be represented as very stable devices having all the characteristics of a series of logic blocks with the exception of showing no increase in delay with a Marginal Inspection voltage applied. Figure fourteen, Section A shows a series of logic blocks paralleled by a delay line and the resulting input and outputs. We can see that in the case of all blocks with nominal delay that we would only be in trouble at extreme limits of marginal voltage,and the failure at this time would most likely be a switching failure. With all ten blocks at worst case delay a slight increase in Marginal Inspection voltage will be sufficient to cause delay failure, but again we are not in trouble because for the worst case delay condition to exist some component within the blocks must be at end of life. Section B of figure 14 is a representation of a short string of logic paralleled by a delay line and demanding coincidence at the output. Here we see our delay safety factor is very small. Increasing our Marginal Inspection voltage toward the limit will most certainly result in delay failure if either block is exhibiting worst case delay at normal voltage. For the worst case delay condition to exist, as in the examble above, requires components, within the block, at end of life.

The only conclusions that can be drawn from this discussion on fixed delays, delay lines and single shots, is that most any conceivable circuit configuration using fixed delays will behave very similar to a circuit which has had the fixed delays replaced by a suitable number of lightly loaded logic blocks.

Delays encountered in I/O devices can run from several milliseconds down to a few microseconds in length. The delays in circuitry which we have been discussing even at worst case have been on the order of millimicroseconds; it is not felt that delays of this magnitude will seriously encroach upon the safety factor usually associated with I/O delays.

Memory delays, or the delays in the core array itself, present a different problem and one which has not been investigated. It is sufficient to say that a cursory examination of the core circuits involved has not shown any particular area in which difficulty could be encountered. Due to lack of information on the effects of Marginal voltage on the core driving circuits and sense amplifiers, some actual circuit evaluations will have to be made before a clear statement on the practibility of Marginal Inspection of memory circuits can be obtained.

FIG. 14


A
1 IN
B1
B2
B3
B4
B5
B6
B7
B8
B9
LATCH
2 IN
200 MYS DELAY LINE
IN 1
IN 2
RANGE IN WHICH SIGNAL COULD FALL
LATCH OUTPUT
SIGNAL WITH NOMINAL DELAY
SIGNAL WITH WORST CASE DELAY
DELAY LINE OUTPUT
DELAY IN MYS
0
50
100
150
200
250
300
IN 1
B1
B2
B
IN 2
40MYS DELAY
IN 1
IN 2
AREA IN WHICH SIGNAL COULD FALL
LOGIC BLOCK OUTPUT
WORST CASE DELAY
NOMINAL DELAY
DELAY LINE OUTPUT
DELAY IN MYS
0
50
100
150

Part III Evaluation of Frequency Variation as a Means of Marginal Inspection

When we increase the frequency of a basic clock in a system, we effectively shorten each clock pulse and simultaneously decrease the overall time cycle of the clock; reducing the frequency of the basic clock has the inverse effect of lengthing the overall cycle and each pulse.

Taking another look at our hypothetical computer, we find that information is advanced from stage to stage by clock pulses 200 millimicroseconds apart. Increasing the frequency of the clock means we are trying to advance information in some time less than 200 millimicroseconds. Any appreciable increase in delay through the ten blocks which make up the stage will cause lack of coincidence on the output and result in failure. Thus by increasing our clock frequency, we have a means of detecting excessive delays. A look at curves one and two on figure nine will show that switching failure may be imminent on a lightly loaded block,and yet delay through this block has not exceeded worst case value. Increasing basic clock frequency may have value in certain areas of the system as a means of detecting excessive delay, but will always have to be augmented by voltage variation to give a true picture of machine condition.

Lowering of the basic clock frequency does not adversely affect most areas of the system if the variation in frequency is kept small. It is not felt that lowering the basic frequency of machine operation has much value as a Marginal Inspection aid. If certain areas of the system prove to be extraordinarily time sensitive, a lowering of basic frequency may allow a greater voltage variation during Marginal Inspection, thus achieving more failure prediction.