SERIES 7000 CIRCUIT MEMO #32

SUBJECT: FERRITE MATERIALS DEVELOPMENT

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ABSTRACT: The work done in exploration of various chemical systems for both high and medium-speed memories is discussed. Results are compared with operating characteristics of materials now in use.

The core driver that resulted from the development program is of a graded base design. Heat sinking of this transistor is accomplished by soldering the collector dot to the metal heat sink structure. Figure 1 is a cross-section of the transistor mounted on the heat sink. The dimensions shown on the section are typical for this device.

The germanium used for the device is processed by standard techniques to the point where material is in the form of a thin wafer of uniform doping of donor impurity for the NPN or acceptor impurity for the PNP. At this point the discussion will become restricted to the NPN for two reasons. (1) The NPN and PNP are similar in many respects and simple comparisons will suffice where applicable, (2) The NPN has proven thus far to be the superior device and has therefore received a much larger amount of development time.

The N doped wafer for the NPN undergoes a diffusion process to form an indium doped skin which produces a P-N junction approximately 0.7 mil from the surface. The indium diffusion is carried out in an evacuated capsule (5 inches long and 1 inch in diameter) which has been back filled with hydrogen to a pressure of 200 mm of Hg. One-half milligram of the indium source was introduced into the capsule with the germanium wafers. Having undergone this heat treatment cycle for diffusion, (the temperature and time are determined by the junction depth desired) the wafers are found to be almost completely P throughout. To remove this condition, the wafers are given a vacuum treatment (16 hrs. at $800^{\circ}C$ in 6×10^{-6} mm of Hg vacuum). This converts them to their original resistivity values and type in the region where diffusion of indium has not taken place. It is with this material that the greatest success was had in making core driver transistors.

After the wafers have received the diffusion and "vacuum bake", they are lapped on one side to a thickness of approximately 3 mils. This produces a wafer which has one surface P type, the other surface N type, the P type surface being of the graded variety. At this point the junction depth is checked by a thermal probe depth gage measurement. The wafers are then cut into 60 mil circular dies by ultrasonic methods.

Prior to making the transistors, the dies are given a pre-etch to remove the high concentration of indium from the "P" type surface. This was found to be necessary to increase the emitter breakdown to acceptable values. The minimum amount of pre-etch needed was found to vary depending on the particular diffusion run used.

To this point the discussion has dealt primarily with the processing of materials prior to making the device. The following discussion will concern itself with a

schedule that produced transistors from this material. Starting with a die of pre-diffused and pre-etched germanium, the following steps were used to make useful devices:

Step 1: The dies are placed in a suitable carrier with a 4 x 15 mil 97% Pb 3% As dot next to the P type surface to form the emitter alloy and a 4 x 40 mil 90% Pb 10% Sb dot next to the N type surface to form the collector ohmic contact.

Step 2: The carrier is then placed in a suitable oven which is maintained at the proper alloying temperature. Figure 2 is a chart showing the firing temperature for various junction depths and amounts of pre-etch for the materials used. The carrier is held in the oven long enough to insure stable temperatures at the desired level and is then removed.

Step 3: The carrier is then placed in an oven which is maintained at a temperature of 710°C for a time of approximately 50 minutes to one hour. This allows a diffusion of the arsenic from the emitter dot into the P type impurity which increases breakdown of the emitter junction.

Step 4: The alloyed dies are then etched to remove any possible N type skin from the P type skin and a nickel washer is bonded to this P type skin. Since this is simply an ohmic base contact, the solder used is a Pb-In alloy which is bonded to the germanium at about 400°C.

Step 5: The units are then mounted on standard headers in the low power dissipation fashion. After etching, the units are tested electrically for their characteristics.

Step 6: Those units which meet core driver specifications are then removed from the standard header and transferred to the heat sink type of base.

Process Yield:

Between step no. 5 and step no. 6 of the processing schedule, the devices are tested and only those meeting the following specifications are considered to be satisfactory core drivers:

Collector to base breakdown voltage, BV_{cBo} at I_c=100 μa >100 V

Emitter to base breakdown voltage, BV_{EBo} at I_e = 100μa >4 V

Punch-through voltage, V_{pt} $\geq$ 100 v

Grounded base frequency cutoff, f_{fco} at I_c = 10 ma $\geq$ 50 mc

Collector current at V_c = 4 v and I_b = 25 ma $\geq$ 500 ma

Saturation voltage drop at I_c = 500 ma $\leq$ 3 v

Base to emitter voltage at I_c = 500 ma $\leq$ 1 v

The yield of devices to the above specifications is as follows:

Total number of starts	167
Number of units rejected	104
Number of units accepted for transfer	63

The percent yield of units considered acceptable for transferring to heat sinks is then 63/167 = 37.7 percent. These units were made in a developmental atmosphere and these yields are, therefore, not representative of a production type of operation.

Of the 63 units that were transferred to heat sinks, there were 53 successful units. This makes the operation of transferring units to heat sinks 84 percent successful. These 53 completed units were then sent to the circuits group for their evaluation. Of the 53, 7 units were found to work satisfactorily in the circuits which means an over-all yield of approximately 4 percent. The majority of these units failed in the circuits for two main reasons. (1) The base current required to produce a 50-millimicrosecond rise time of collector current exceeded the 50-ma limit set by the circuits group and (2) The saturation voltage was found to exceed the tolerance set by the circuit application.

The PNP is made in a similar manner to the NPN with one exception. This exception is the manner in which the effective graded base is formed and base width is controlled. The steps in making the PNP are as follows:

Step 1: The material is prepared in a manner similar to the NPN with the impurity types interchanged, and the junction depth not as deep. Since the body of the material is "P" type, the difficulties with thermal conversion are not experienced with wafers for the PNP and therefore do not receive the extra vacuum baking step.

Step 2: The collector and emitter are alloyed in a manner similar to the NPN with the exception that the emitter dot contains both "P" type and "N" type impurity in a suitable metal carrier. The

impurities are chosen on the bases of their segregation coefficients and diffusion coefficients, the object being to have the "N" type impurity to diffuse ahead of the "P" type region resulting from the "P" impurity and the segregation of the "P" impurity to be greater than the "N" type to form the "P" type emitter region.

The remaining steps of bonding washers, mounting, testing and transferring to heat sinks are identical to the NPN with the impurity types interchanged where applicable.

The process for making the PNP is more attractive than that for the NPN because of the possibility of maintaining better control of base width. However, the development was not carried very far because the NPN proved to be a faster device, had lower saturation voltage and produced fewer thyratrons (alphas greater than unity).

For these reasons, it was considered that the best chance of obtaining a suitable core driver in the time required lay with the NPN.

As a summary of the results of the PNP development the following statements can be made:

(1) The PNP process produced about 20 units which were considered satisfactory to be sent to the circuits group.

(2) These 20 transistors were found by the circuits group to require more than the allowed base current to produce 50 m s rise time and the saturation voltage was more than the circuit would tolerate. This means that no PNP transistors were produced that were acceptable in circuit operation.

(3) The PNP process produced a large percentage of units which had alphas which were greater than unity in the desired current range. This condition is a variable in the sense that it did not occur at the same current or voltage level in the transistors and the level at which it did occur would change in individual transistors. This inherently means that the confidence figure is low for the PNP core driver. That is to say, a transistor which does not show this effect in the range in which it was tested may have this effect present outside this range. Considering the experience that the level at which this does occur tends to decrease when there is a change means that it is very possible that a transistor may show an alpha greater than unity during operation even though this effect did not show in normal testing.

To summarize the development program, a list of conclusions and recommendations follow:

(1) The yield of acceptable NPN units for transferring to head sinks is reasonably good. The yield of NPN units acceptable in circuit use is very poor. Even though this over-all yield is poor, it does indicate that NPN transistors can be made that will meet circuit requirements. From this consideration, a reasonable amount of confidence can be maintained that further development on the NPN will result in a device which will have a reasonable over-all yield.

(2) The PNP process did not produce acceptable units for the circuit application. Therefore the possibility of producing a PNP transistor to match the NPN core driver transistor is discouraging. However, a thorough understanding of the PNP core driver transistor may lead to solutions circumventing the shortcomings of this device.

It is therefore recommended that the development program for the NPN core driver be continued to the point where a satisfactory yield can be realized for this device, and that a study program for the PNP core driver be instituted to investigate the reasons for its shortcomings.

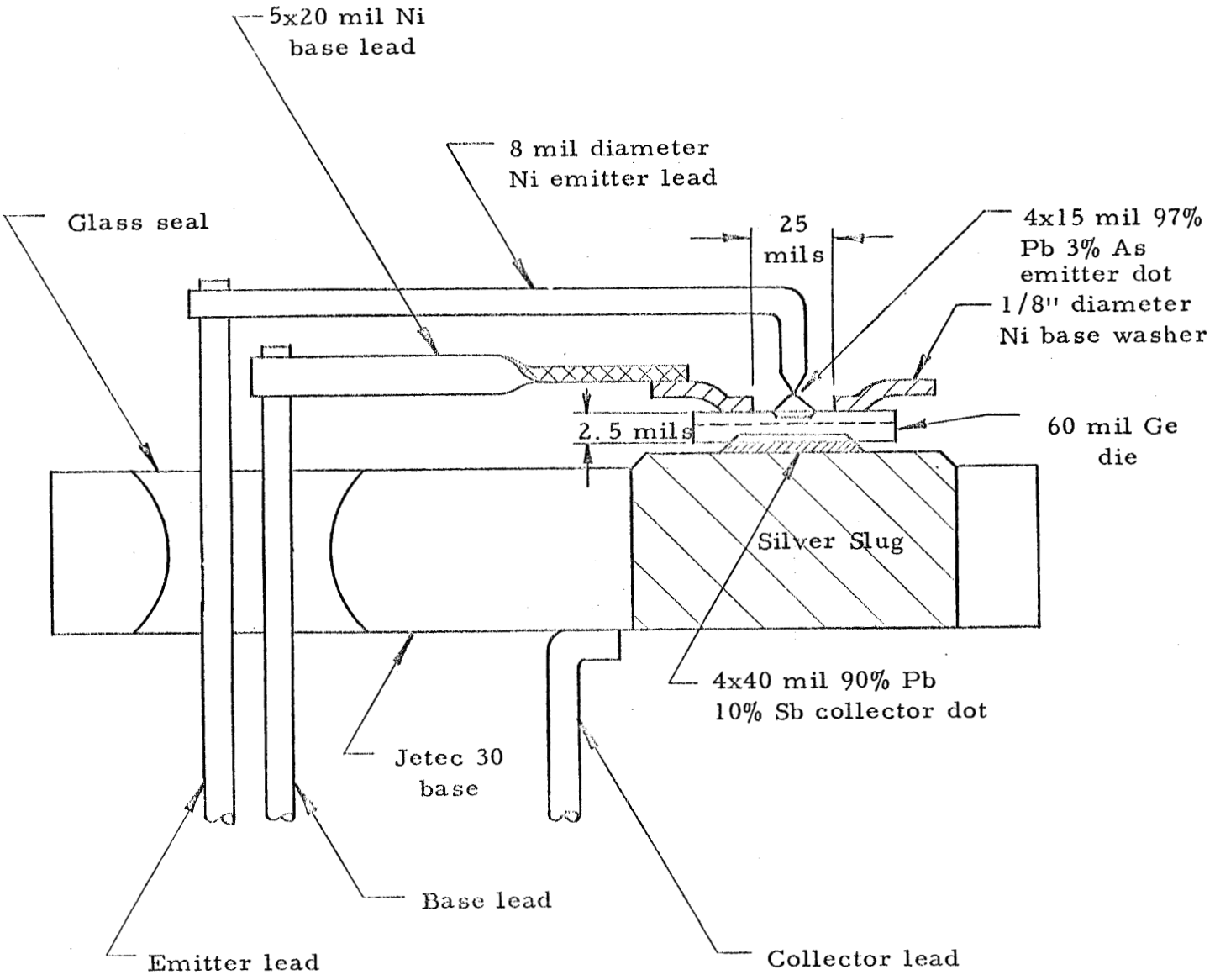
5x20 mil Ni
base lead
8 mil diameter
Ni emitter lead
Glass seal
25
mils
4x15 mil 97%
Pb 3% As
emitter dot
1/8" diameter
Ni base washer
2.5 mils
60 mil Ge
die
Silver Slug
4x40 mil 90% Pb
10% Sb collector dot
Jetec 30
base
Base lead
Emitter lead
Collector lead

FIGURE 1.

Junction Depth Mils	Pre-Etch Sec. CP 8	Alloying Temp. °C
0.7	10	725
etched to 0.7	none	740
0.8	15	740
etched to 0.8	none	740
0.9	15	745
0.9 low concentration "P" surface	none	760
1.0 no etch	15	755

FIGURE 2