SERIES 7000 CIRCUIT MEMO #29

SUBJECT: PROPOSED SYSTEM DESIGN FOR THE HIGH-SPEED MEMORY

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DATE: August 30, 1957

ABSTRACT: This report concerns the full-size memory design of a 1024-word, 72-bit high-speed memory.

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I. GENERAL DESCRIPTION OF MEMORY ARRAY

A. Memory Element

1. Three hole biased multi-path core
2. 1.1 amp (nominal) per drive line
3. Element wiring - Figure 1

B. Memory Size

1. 1024 Words
2. 72 Bits per word
3. X-Y Drive Segmenting - Figure 2
4. Sense Segment (four per plane) 16 x 16 cores
5. Inhibit Segment (four per plane) 16 x 16 cores

C. Plane Size

1. Four segments of 16 x 16 cores
2. Each segment 5-5/8" x 5-5/8" (includes frame)
3. Packing Density - approximately 6 cores/inch in each segment

D. Drive Currents

1. X-Y Current furnished from Matrix Switch

    a. 1.1 amp nominal
    b. Rise Time = 40 mus, Flat Top = 80 mus
       Fall Time = 40 mus (all nominal)
    c. Array X-Y Drive Delay = 75 mus

I. D. Drive Currents (Continued)

2. Inhibit currents furnished from direct drive transistor drivers

a. 1.26 amp nominal
b. Rise Time = 40 mus nominal
Flat Top = 220 mus nominal
Fall Time = 40 mus nominal
c. The Inhibit Drivers will be staggered in turning on. That is, the Z Driver in the first plane will turn on before the Z Driver for the 24th plane.
d. Since there are four Z segments per plane, the memory is designed so that only 1/4 of the Z drivers needbe turned on during a memory cycle.
e. Array Z delay = 25 mus

E. Sense

1. One Sense amplifier per plane

a. Four Sense segments per plane with 16 x 16 cores each
b. Sense Amplifier discriminates between a 260 mv "one" and a 100 mv "zero"

2. The sense amplifiers require a strobe pulse during the "read" portion of a "Read from Memory" cycle.

3. The strobe pulse is time delayed down the memory planes to take into account the drive delay.

F. Array Delay

1. X-Y Delay - 75 mus (32 x 24 cores)

2. Inhibit Delay - 25 mus (16 x 16 cores)

3. Sense Delay - 25 mus (16 x 16 cores)

G. Array Timing Cycle

1. Figure 3

II. DESCRIPTION OF MEMORY LOGIC

A. Recognition of Memory and Start Memory Cycle Logic

1. The Central Control Unit (C. C. U.) in the Bus provides memory recognition and triggers the memory timing ring. The memory sends back a busy signal to the C. C. U. This busy signal is reset when the memory can accept a new address, allowing for transmission time of the signal to the C. C. U. and for data back to the memory.

B. Memory Address Register

1. The Memory Address Register (MAR) gates are controlled by the bus. The 11 gates open and allow the MAR to set up to the configuration supplied by the bus. The MAR is reset during the write portion of the cycle. At this time the memory is free to accept new information.

C. Memory Address Decoder

1. Figure 4 shows the winding pattern of the 32 input, 16 output matrix switch. The 32 inputs are grouped in pairs of drivers so that there are a total of 16 pairs of drivers for each matrix switch. During the read portion of the memory cycle, one driver out of each pair turns on. During the write portion, the other half of each driver pair turns on. The 16 drivers which turn on during read time add power to switch the selected matrix switch core. All other cores receive no effective current due to cancellation. During the write portion, the other 16 drivers turn on to reset the matrix switch core. Refer to STM-14.

II. C. Memory Address Decoder (Continued)

Figure 5 shows the logical functions which were derived from the winding pattern of the matrix switch. These logical functions select which output of the matrix switch is energized.

Figure 6 shows the basic decoder which is used to provide the necessary logical functions for either X or Y dimensions.

The MAR contains the address of the word in memory. Four bits of this address are used for X decoding and four bits for Y decoding. Bits A, B, C, D and their complements (Figure 7) are sent to the "Exclusive Or's" in the manner shown and the logical functions are generated. These functions along with the information bits A, B, C, D, $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$ are then brought to the "Switching Exclusive Or's" where they are "exclusive ored" with the output from the Read/Write, flip-flop. The Read/Write (R/W) flip-flop is true for read time and false for write time. This flip-flop causes the outputs of the "Exclusive Or's" to switch when it changes state. The outputs of the "Switching Exclusive Or's" are tied to driver gates, where they are "anded" with the matrix switch selection outputs. The proper gates are opened to turn on sixteen drivers during the read portion of the cycle. After "read" time the R/W flip-flop changes its state thereby changing the output of the "Switching Exclusive Or's" at "write"time. The outputs are sampled at the driver gates by the matrix switch selection line and the remaining 16 drivers of the 16 pairs are turned on.

D. Matrix Switch Selection

1. In Figure 8, the two high order bits (J, and K) of the memory address were used to select which matrix switch was to be energized. This does not necessarily have to be so, in that by using the low order bits for this purpose, the word locations within a memory unit can be staggered. For instance; bit A could be used to select one of the X matrix switches and bit B could be used to select one of the Y matrix switches. This would stagger sequential addresses throughout the memory unit.

II. D. Matrix Switch Selection (Continued)

2. Selection Logic

Bits J and K are used to define left and right X and Y matrix switches respectively. The four possible combinations of J and K are obtained by "anding" the normal and complement outputs from each of these bits with a timing pulse in four sets of "And" circuits. Since only two of these "And" circuits can be true at one time, only one X and one Y matrix switch will be selected. The length of time the drivers are on for the "read" and "write" portions of the memory cycle is also set by the timing pulse with which the matrix switch selection bits are gated.

E. Regenerate and Store Logic

1. Regenerate

In a "Read" cycle, the memory user is requesting data from the memory. This also means that the memory has to retain the data for any future references. The "read" portion of a memory cycle destructively reads the data out of the cores which, in conjunction with what was stated above, implies that the same data taken from memory must be written back into the memory location as well as being sent to the memory user. This is done by a regeneration loop.

The memory user sends an address to memory where it is decoded and the proper X and Y drivers are turned on. The selected matrix switch cores send half-select currents down the selected X and Y drive lines. The cores which receive a full select switch (if they are in "one" state) and induce voltages in the sense wires. The voltage is amplified by the sense amplifiers (S.A) and the data register is set up to the configuration of the word which was just "read."

II. E. Regenerate and Store Logic (Continued)

1. The true sides of the data register flip-flops are gated to the output bus. The complement sides are gated with the inhibit segment select line and staggered timing pulses. The outputs of the gates are sent to the inhibit drivers. The inhibit drivers connected to the planes in which "zeros" were stored are turned on. This provides half-select pulses which are of opposite polarity to the "write" current thereby cancelling out one of the "write" half-selects and preventing the writing of a "one" into the core.

   No Post Write Disturb Pulse is required in this memory since the memory element is d-c biased.

   The logic for the selection of the inhibit segments is shown in Figure 9. Bits J and K are used to determine which segment should be turned on. The four possible combinations are "anded" together as is shown and provide signals to the inhibit gates.

2. Store

   In a "Write" cycle the memory has to store new data into a memory location. The C.C.U. sends the memory a recognition pulse, the memory address, the data to be stored, and a store pulse. These are gated into the memory by the bus. The memory decodes the address and turns on the X and Y drivers. The data is sent to the data register. The store pulse sets the store flip-flop to its false state and prevents the strobe pulse from turning on the sense amplifiers. It also prevents the data from being gated to the output bus. During the "write" portion of the cycle, the proper inhibit drivers are turned on, in the manner described above, thereby writing the new data in the memory location.

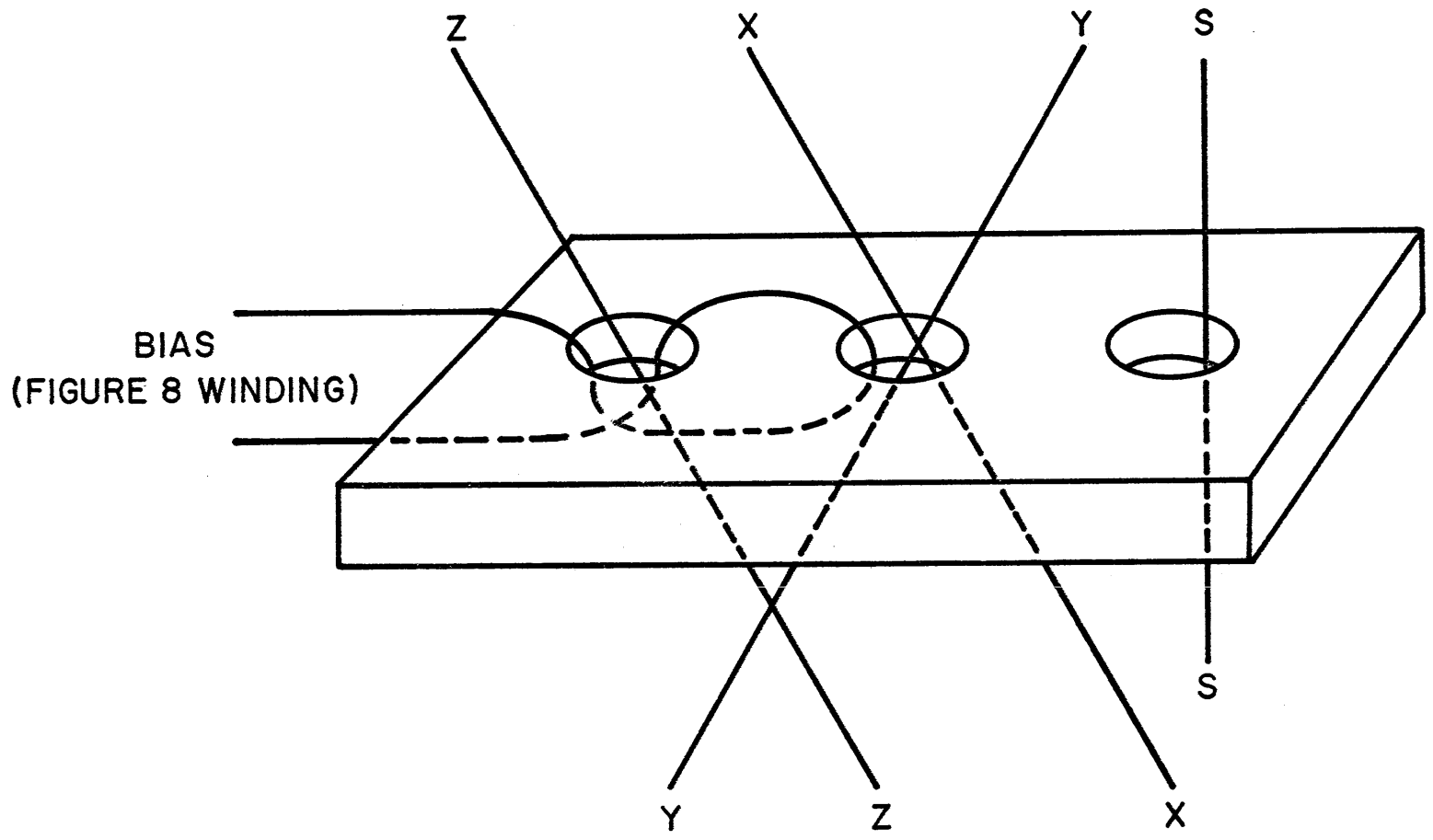
II. F. Special Features

1. Parity Checking

The memory address is parity checked. The bus supplies the parity bit as well as the ten address bits to the memory. The memory address and the parity bit are sent to the parity checking logic (Figure 8) for comparison. If there is an error the signal is gated to the alarm circuit.

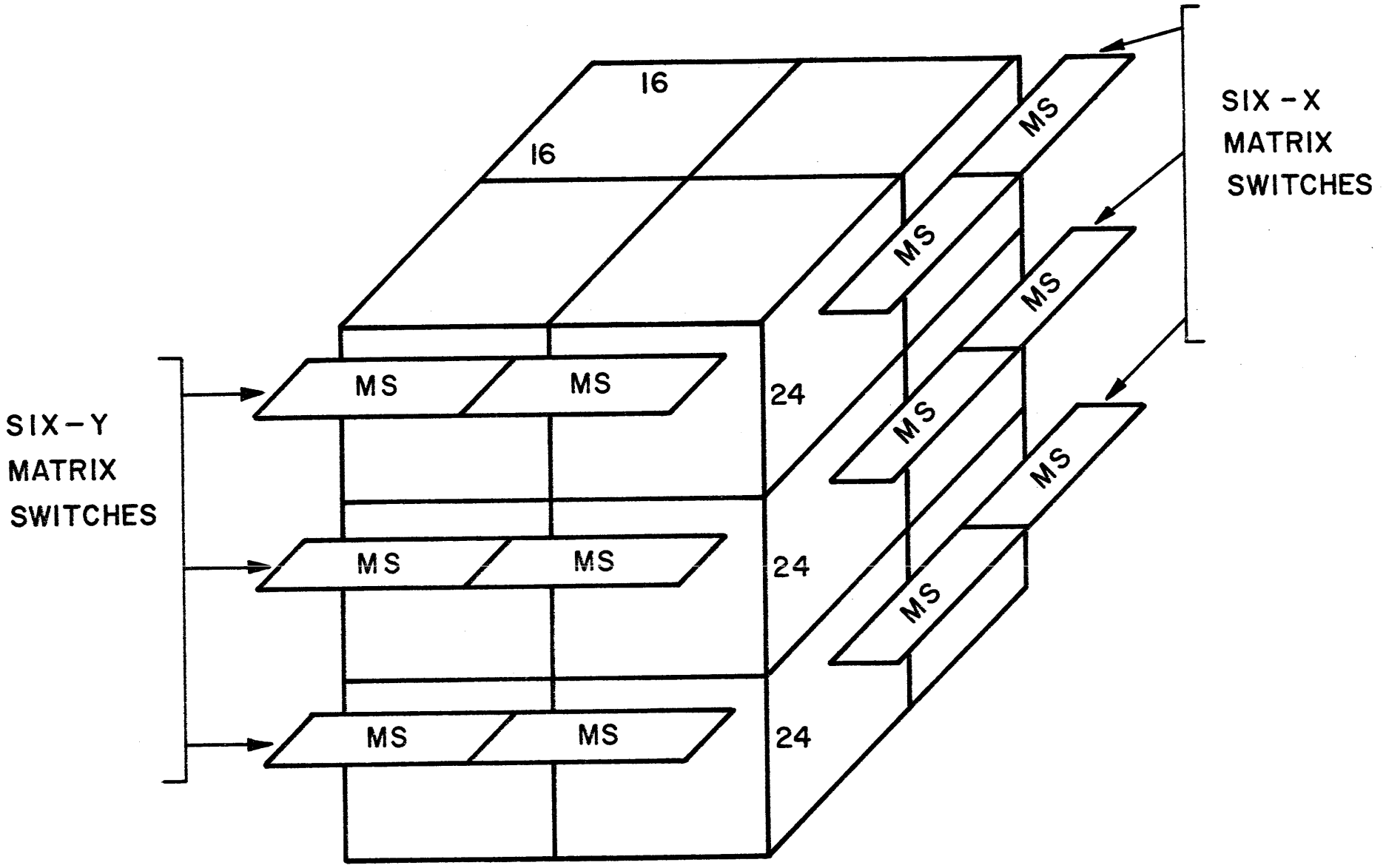
2. Address Checking

The Address Checking encoder described in Silo Technical Memos 16 and 28 is also used in this memory as is indicated in Figure 8.



X & Y ARE WORD SELECT DRIVE LINES
Z IS THE INHIBIT DRIVE LINES
S IS THE SENSE WINDING

FIGURE I ELEMENT WIRING



X-Y DRIVE SEGMENTING

FIGURE 2

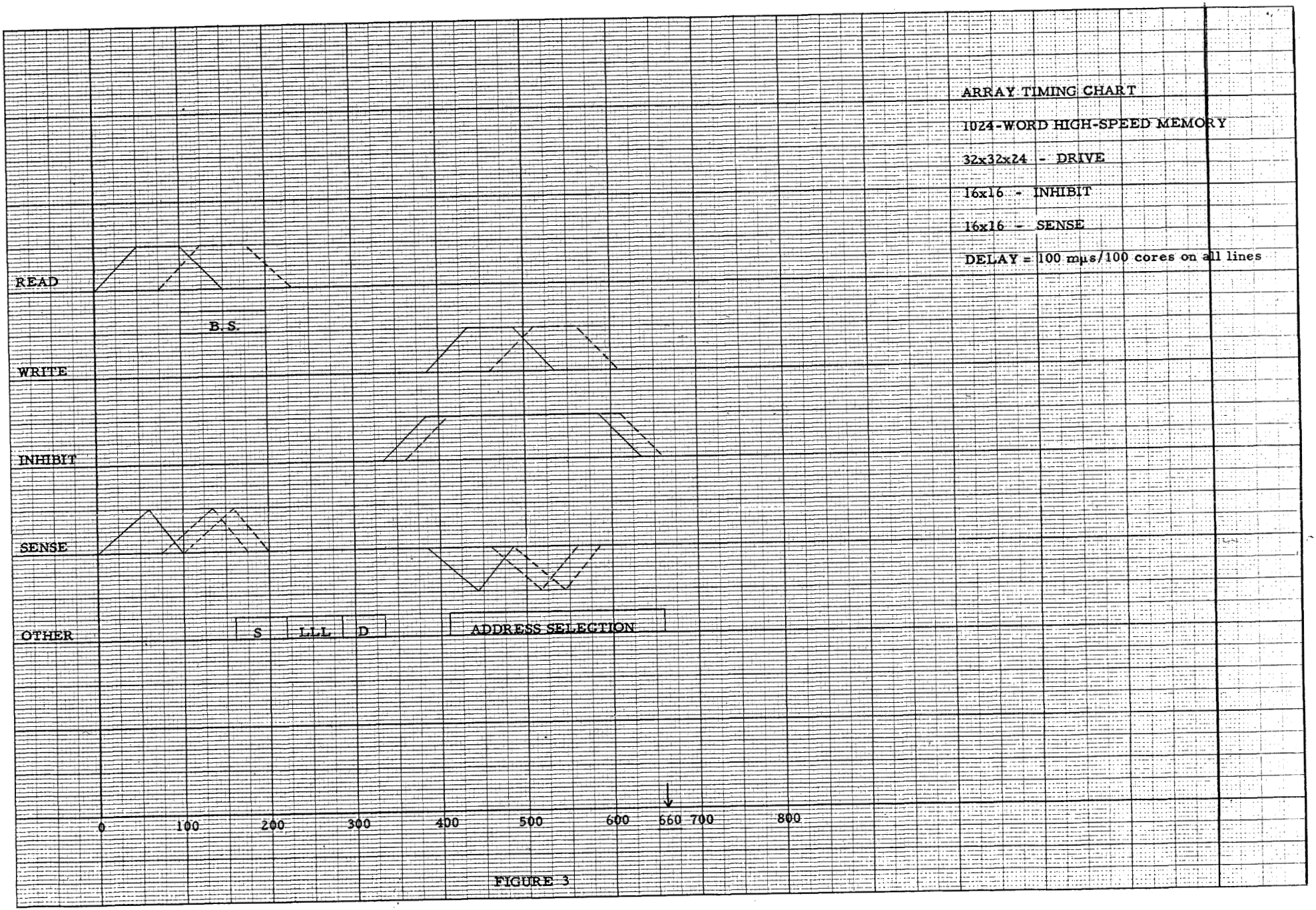

ARRAY TIMING CHART
1024-WORD HIGH-SPEED MEMORY
32x32x24 - DRIVE
16x16 - INHIBIT
16x16 - SENSE
DELAY = 100 mμs/100 cores on all lines
READ
B.S.
WRITE
INHIBIT
SENSE
OTHER
S
LLL
D
ADDRESS SELECTION
0
100
200
300
400
500
600
660
700
800

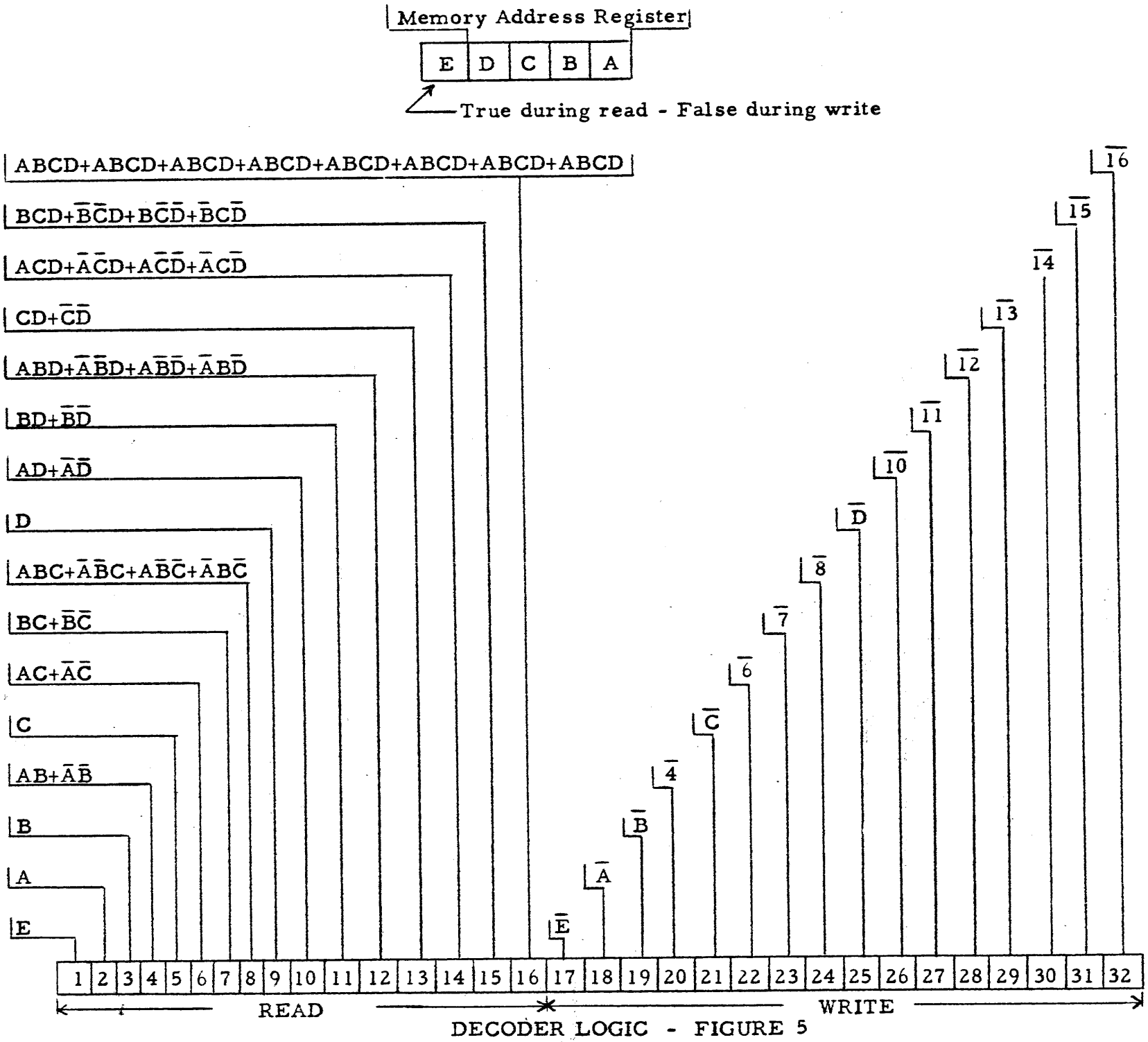
FIGURE 3

INPUTS

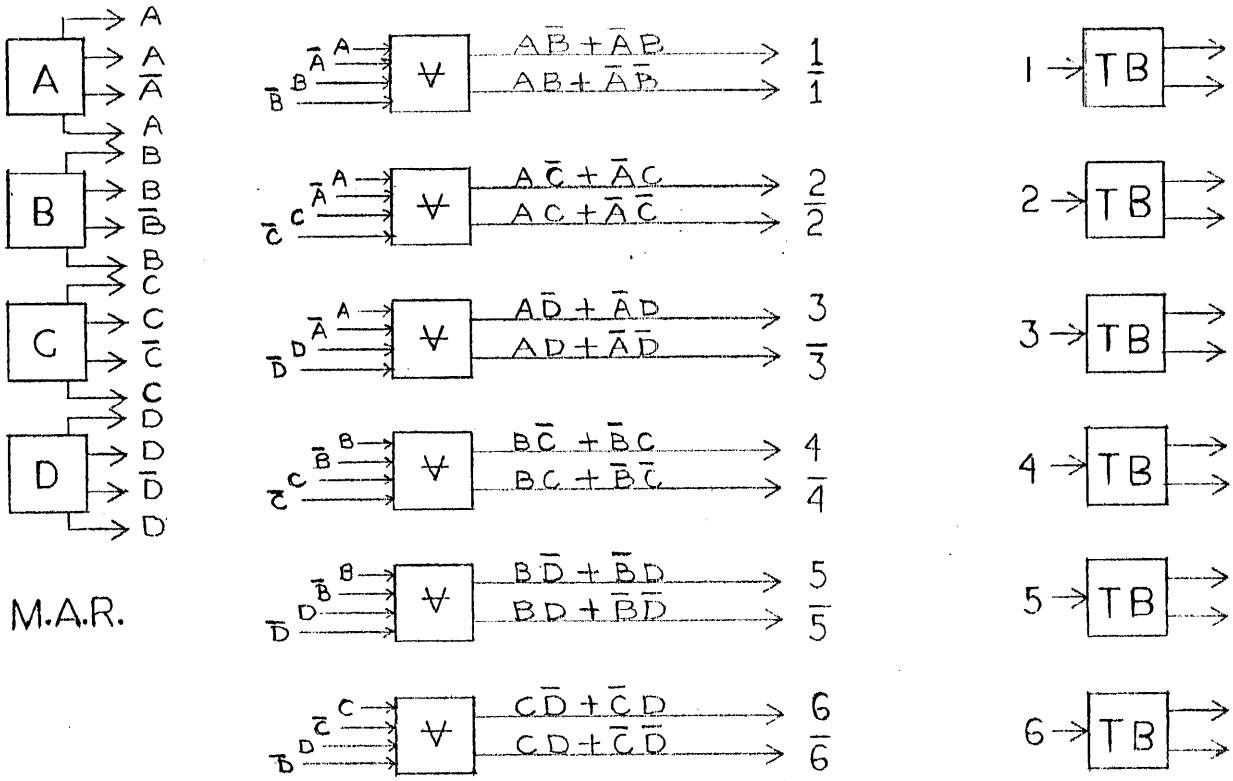
OUTPUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
I	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
II	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
III	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
IV	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
V	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
VI	1	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1
VII	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
VIII	1	0	0	1	0	1	1	0	1	0	0	1	0	1	1	0
IX	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
X	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1
XI	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1
XII	1	0	0	1	1	0	0	1	0	1	1	0	0	1	1	0
XIII	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
XIV	1	0	1	0	0	1	0	1	0	1	0	1	1	0	1	0
XV	1	1	0	0	0	0	1	1	0	0	1	1	1	1	0	0
XVI	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

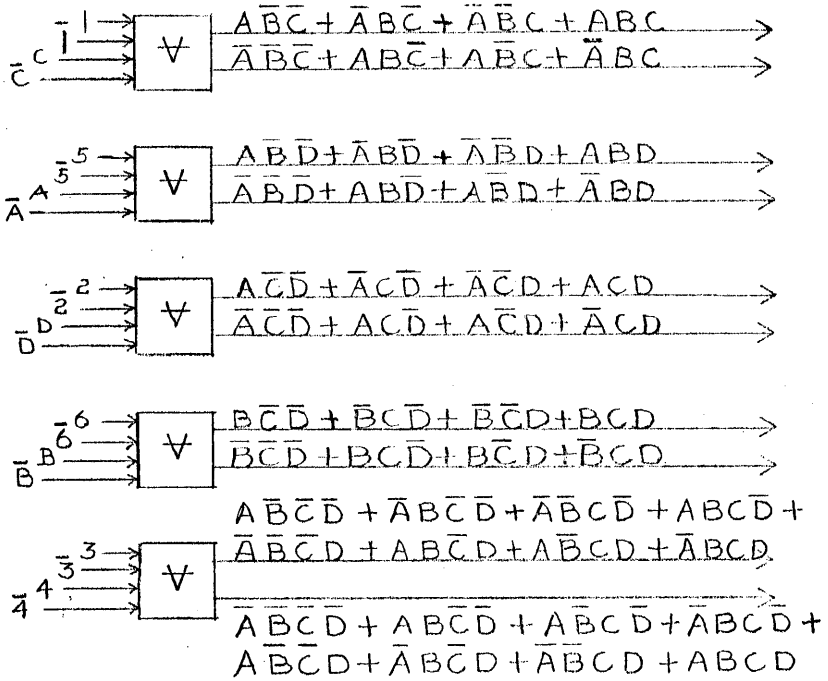
MATRIX SWITCH WINDING PATTERN

Figure 4



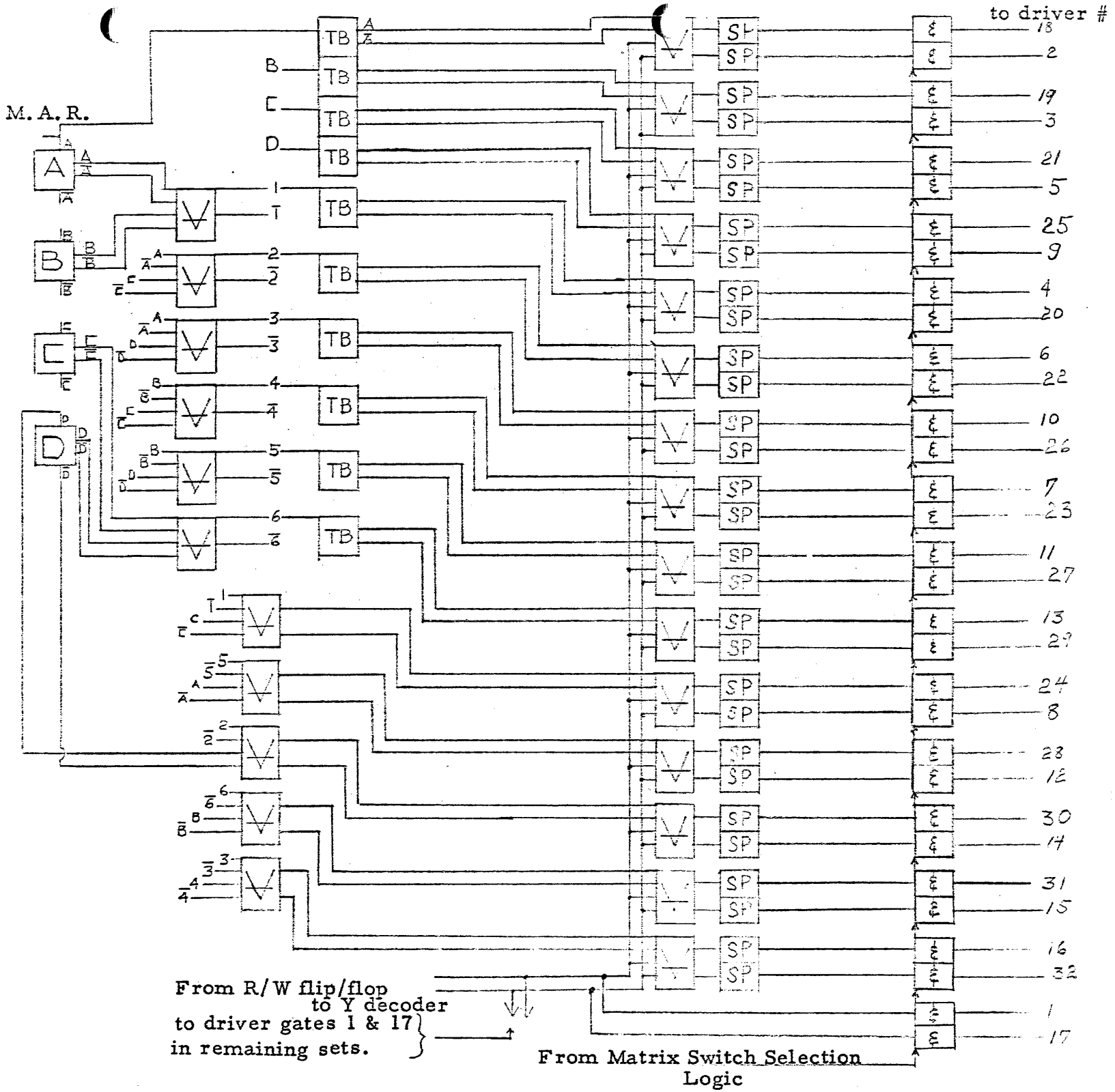
DECODER LOGIC - FIGURE 5





DECODER FOR A 16 OUTPUT MATRIX SWITCH

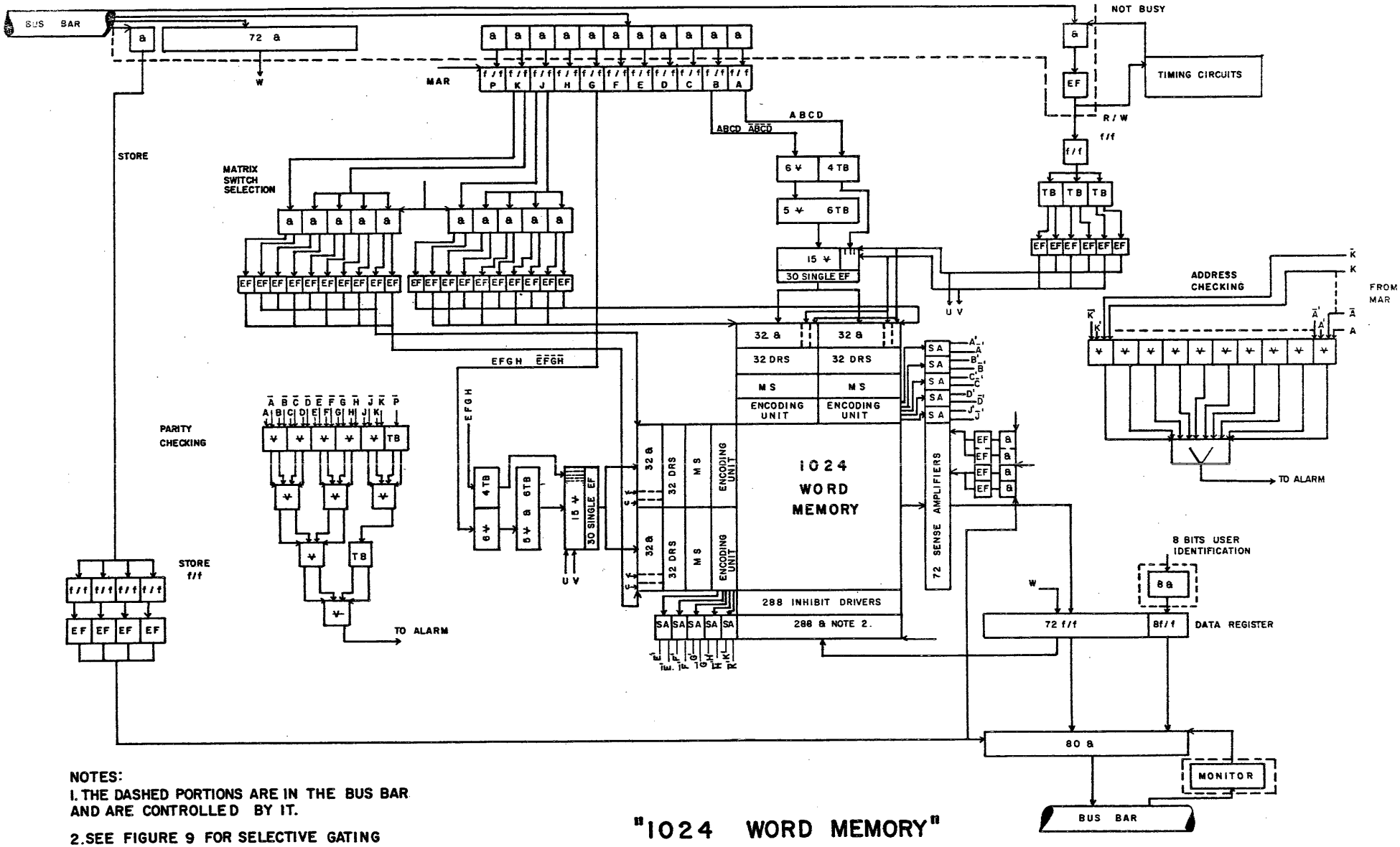
FIGURE 6



The outputs from SP's also go to the appropriate driver gates in the remaining sets of drivers.

X DECODER LOGIC AND SWITCHING CIRCUITS

FIGURE 7



NOTES:
1. THE DASHED PORTIONS ARE IN THE BUS BAR AND ARE CONTROLLED BY IT.

2. SEE FIGURE 9 FOR SELECTIVE GATING OF INHIBIT DRIVERS.

"1024 WORD MEMORY"
FIGURE 8

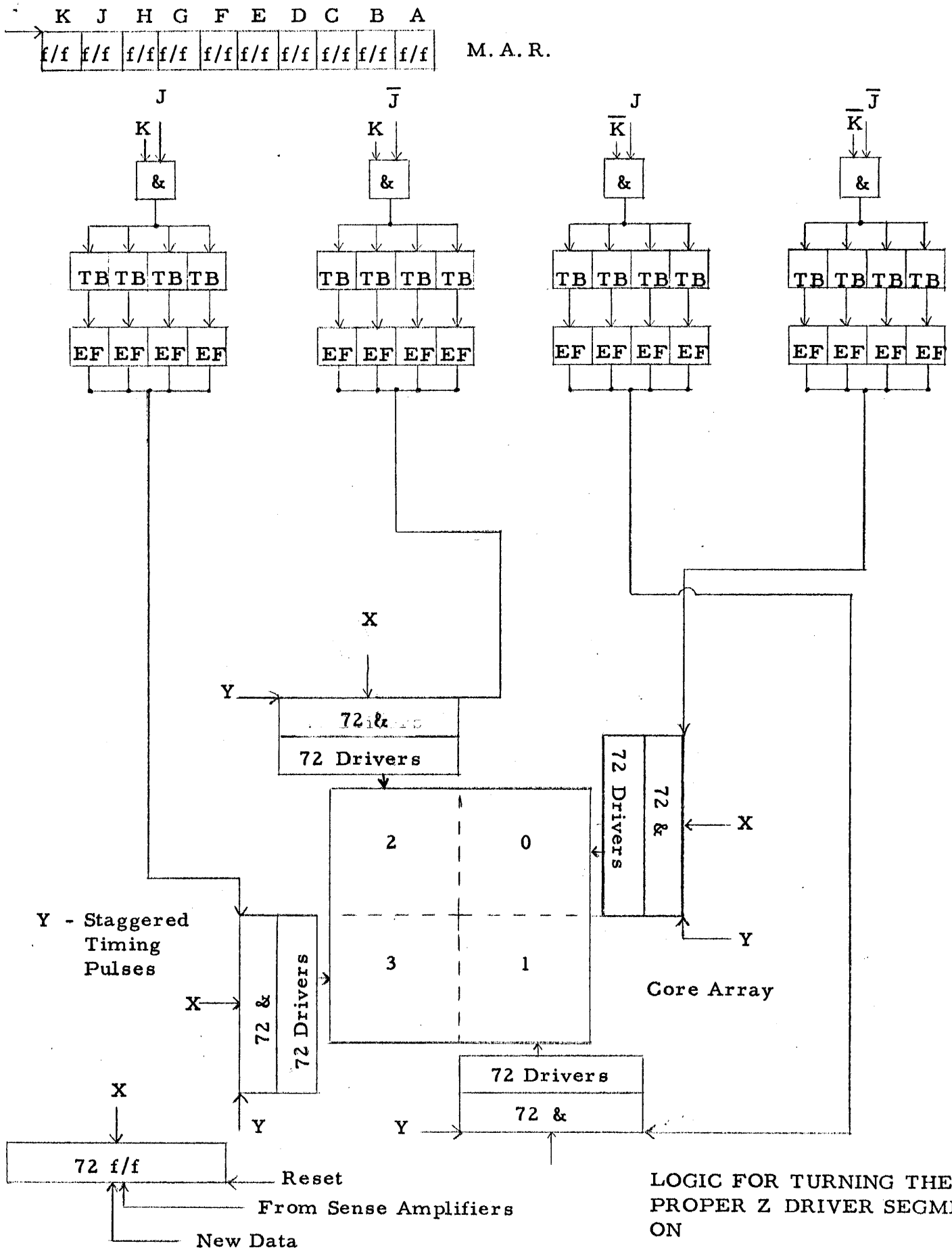

K J H G F E D C B A
f/f f/f f/f f/f f/f f/f f/f f/f f/f f/f
M. A. R.
J
K
&
TB TB TB TB
EF EF EF EF
J
K
&
TB TB TB TB
EF EF EF EF
J
K
&
TB TB TB TB
EF EF EF EF
J
K
&
TB TB TB TB
EF EF EF EF
X
Y
72 &
72 Drivers
72 Drivers
72 &
X
Y
2
0
3
1
Core Array
Y - Staggered Timing Pulses
X
72 &
72 Drivers
Y
X
72 f/f
Reset
From Sense Amplifiers
New Data
72 Drivers
72 &
Y
LOGIC FOR TURNING THE PROPER Z DRIVER SEGMENT ON

FIGURE 9.