SERIES 7000 CIRCUIT MEMO #20

SUBJECT: CORE TESTING METHODS AND EQUIPMENT

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ABSTRACT: This report describes the methods and equipment associated with testing toroids and multipath structures. The problems that have been encountered and their solutions, when known, are discussed.

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I. INTRODUCTION

This report describes the methods and equipment associated with testing toroids and multipath structures. The problems that have been encountered and their solutions, if known, are discussed.

Experimental lots of 30-50-12 mil toroids are being evaluated in quantities using the present automatic handlers with only minor modifications.

The majority of the mechanical problems associated with 3-hole core testing have been eliminated, but some electrical problems still exist.

Core testing has imposed special requirements on the electrical testing equipment due to the fast rise time of 50 mμs and the high repetition rate of 2 Mc. Because commercial test equipment is not available to meet these requirements, it has been necessary that this project develop and construct the majority of its core testing equipment.

The construction of the equipment described in this report was financed by IBM. It is described here because a considerable portion of the development work on the equipment was done on Project SILO.

II. CORE TESTING METHODS

The general purpose of this section is to describe the equipment and problems directly associated with core testing, and their solutions if known.

Testing of 30-50-12 Toroids

The testing of 30-50-12 mil toroids is quite similar to testing of 50-80-25 toroids. A slight modification of the track and probe assembly on a 50-80-25 automatic core handler permitted the handling of the smaller core. A two-conductor probe, 0.020" in diameter, is used in testing the cores (see Figure II-1).

II. (Continued)

For small-lot evaluation, a cam rack logic unit is being used in conjunction with a "relay-condenser" type driver. Currently under development is a hard tube driver to operate with the driver logic unit described in the section on the Driver Logic Unit.

3-Hole Core Handlers

For testing small quantities of 3-hole cores, a small jig was constructed which tests only one core at a time. (See Figure 1F in the section on the Fast Rise Time Thyratron Driver.) An important feature of this jig, over previous ones, is the wiping contacts which minimize contact resistance. The entire jig can be emersed in Freon to eliminate any heating problems, and to duplicate the conditions expected in the final machine.

For testing large quantities of 3-hole cores, a Syntron-type automatic handler has been constructed (see Figure II-2). It is essentially the same as the 30-50-12 handler except that the cores slide down the track on their long axis, instead of rolling. The probe assembly is constructed so that one single-conductor probe passes through each of the three holes (see Figure II-3). This probe, after passing through the core, enters a wiping type contact which can be divided into three separate contacts (see Figure II-4). These separate contacts give the versatility desired for the investigations to be mentioned later. The wiring diagram of the handler, Figure II-5, shows the circuits used to give reliable accept/reject operation and provide protection for the probes.

Pulse Width Problem

Data concerning the pulse width problem has been obtained which indicates a deterioration in the 1:0 ratio to approximately 2.5 to 3:1 as the pulse width narrows to 150 mμs. Significant curves are shown in Figure II-6. Recent experiments indicate that the reduction in the 1:0 ratio is due to incomplete switching at the narrower pulse widths. Differences between the two graphs are due to the difference in the impedance of the bias supplies used and the difference in drive-current leading-edge shapes. The discrimination capabilities of the sense amplifiers will determine the magnitude of the problem, if any.

II. Bias Heating

Because of the large direct currents used in biasing the cores, any small resistance results in a relatively large amount of power being dissipated as heat. As mentioned above, the small 3-hole core testing jig can be placed in a bath of Freon to virtually eliminate the effect of bias heating. With the automatic handler, however, the use of Freon is not feasible, and some other scheme is required. One method would be to use pulse bias, i.e., to turn the bias on before a read or write pulse, and off after the read or write pulse is down. This would be difficult, since the bias currents in the Z-hole and the center hole must turn on and off coincidently. A thyratron driver would be required that is capable of generating a 3-amp current pulse, and calibration of the bias pulses in each leg would be required.

Another approach suggested for the solution to this bias heating problem is that of testing the 3-hole core like a toroid. In this case there would be no bias, the core being driven only in the center hole with read-write pulses. Both outside holes could be sensed, eliminating the need for interchanging the bias and sense holes as mentioned below. The data from this method would have to be correlated with the ordinary method of testing.

Bias Supplies

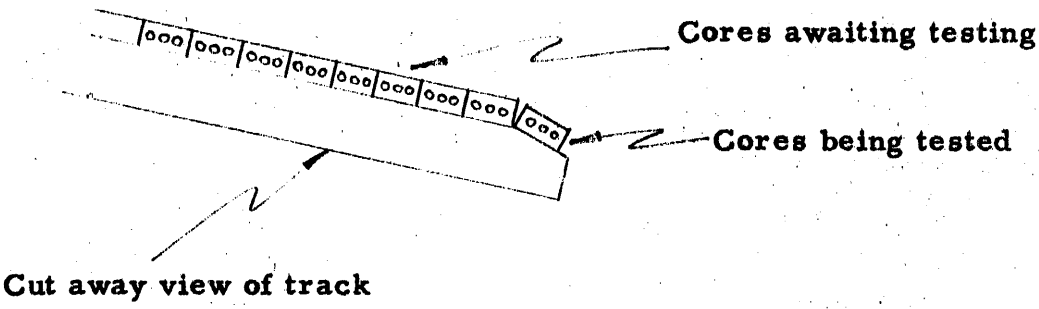
A recent investigation concerning the correlation between various setups resulted in replacing the low-voltage high-current bias supplies with high-voltage high-current supplies. The resulting increase in the bias impedance by a factor of 10 resulted in a much closer correlation of data. This type of bias supply does present a problem in that it is necessary to provide some sort of protection circuit to insure that the bias is off before the probes pull away from their contacts. A relay to provide this protection is shown on the wiring diagram of the automatic handler (Figure II-5). If this protection were not provided, the life of the probes would be very short due to the tendency for arcing.

Butting Problem

In the automatic handler there is what is known as the butting problem. This occurs when the cores waiting to be tested slide down the track and

II. (Continued)

come in contact with the core being tested. If this butting occurs on the bias side, the operation of the core being tested is virtually destroyed. On the other hand, if the butting occurs on the sense side, the output of the core is somewhat increased. This problem is also present in the 3-hole-toroid approach. The solution to this problem is being attempted by machininga slight angle in the track so that the cores come in contact only on one corner, as shown below.



Cut away view of track

Flash

Flash is the buildup of material along the edges of the 3-hole cores, primarily due to wear in the pressing tools. Although this flash only projects 0.002" chipping it from the region of the sense hole results in the "one" output decreasing about 8%, and the "zero" and switching times increasing slightly. This flash must be kept at a minimum since its presence represents a direct possibility of a good core becoming bad during the winding process.

Complete Testing

Until a core is wired in a plane, there is no distinction between the sense and bias holes. For this reason, the core would have to be tested

II. (Continued)

twice, interchanging the sense and bias holes between tests. A proposed system has been worked out which will switch the bias and sense probes. Before further work can be done on this phase, a satisfactory solution to the bias heating problem must be found.

Here again the toroidal approach to 3-hole core testing would be advantageous, since it would eliminate the need for reversing the probes. Both outside probes would now be sensed at the same time.

Calibration

A significant problem associated with both toroid and 3-hole core testing is the problem of calibration. Several schemes have been investigated, with three methods now undergoing consideration. The simplest and least accurate is the use of an oscilloscope and its amplifier to compare the unknown pulse with a known step function. Another method involves using direct deflection in a cathode-ray tube, and an accurate direct current potential for positioning. The third scheme is to generate a pulse of known height and similar shape to the unknown pulse, and comparing these in a differential amplifier.

Conclusion

In testing the 30-50-12 toroids, the similarity between these and the 50-80-25 toroids makes possible the use of the 50-80-25 toroid testing equipment and procedures, with only minor refinements.

Testing the 3-hole core, however, offers many new and different problems over those previously encountered in toroid testing. Many of these problems have already been solved, and the others are currently under investigation.

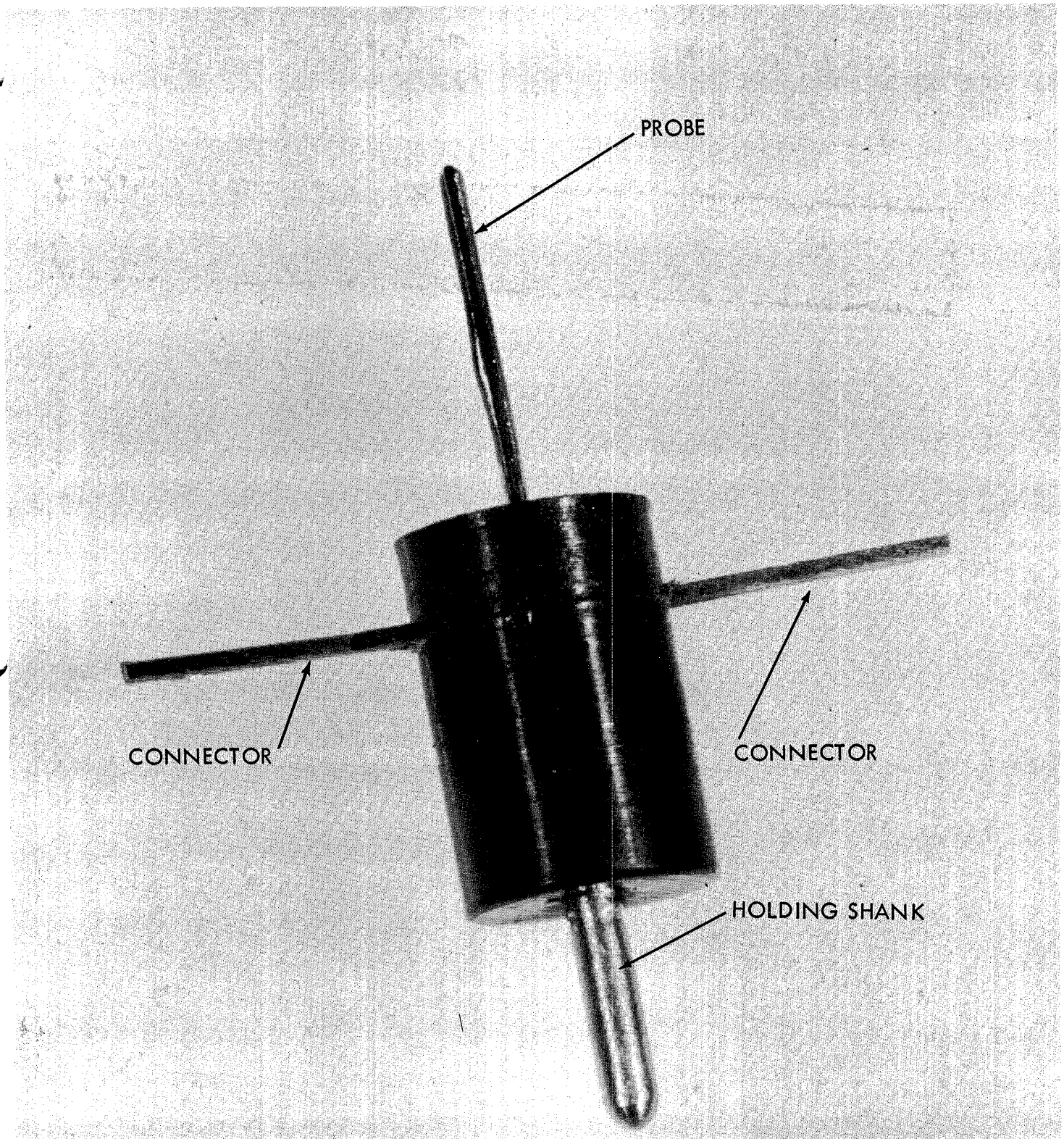


FIGURE 1 TWO CONDUCTOR PROBE FOR 30-50-12 TOROIDS

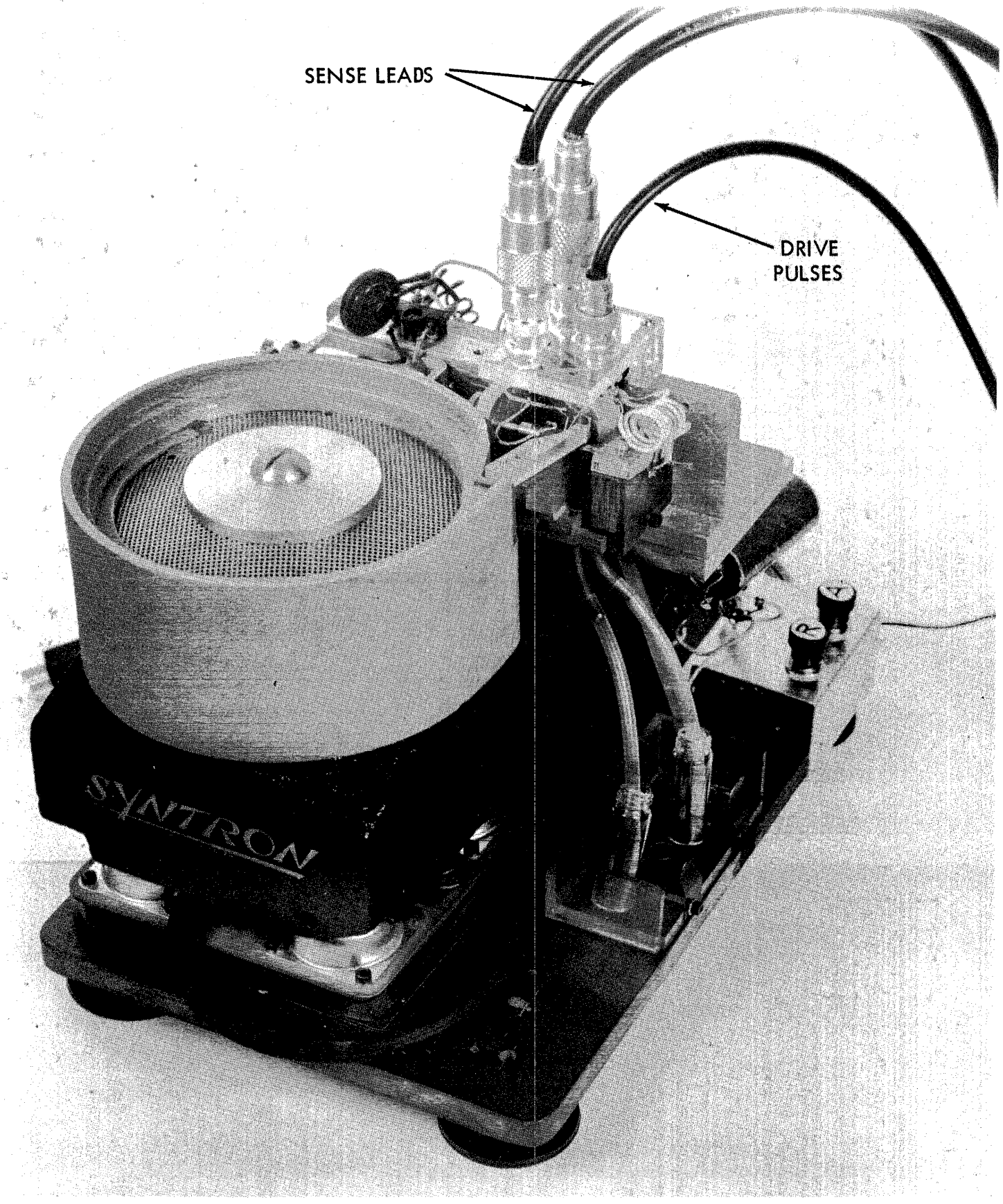


FIGURE 2 - AUTOMATIC 3-HOLE CORE HANDLER

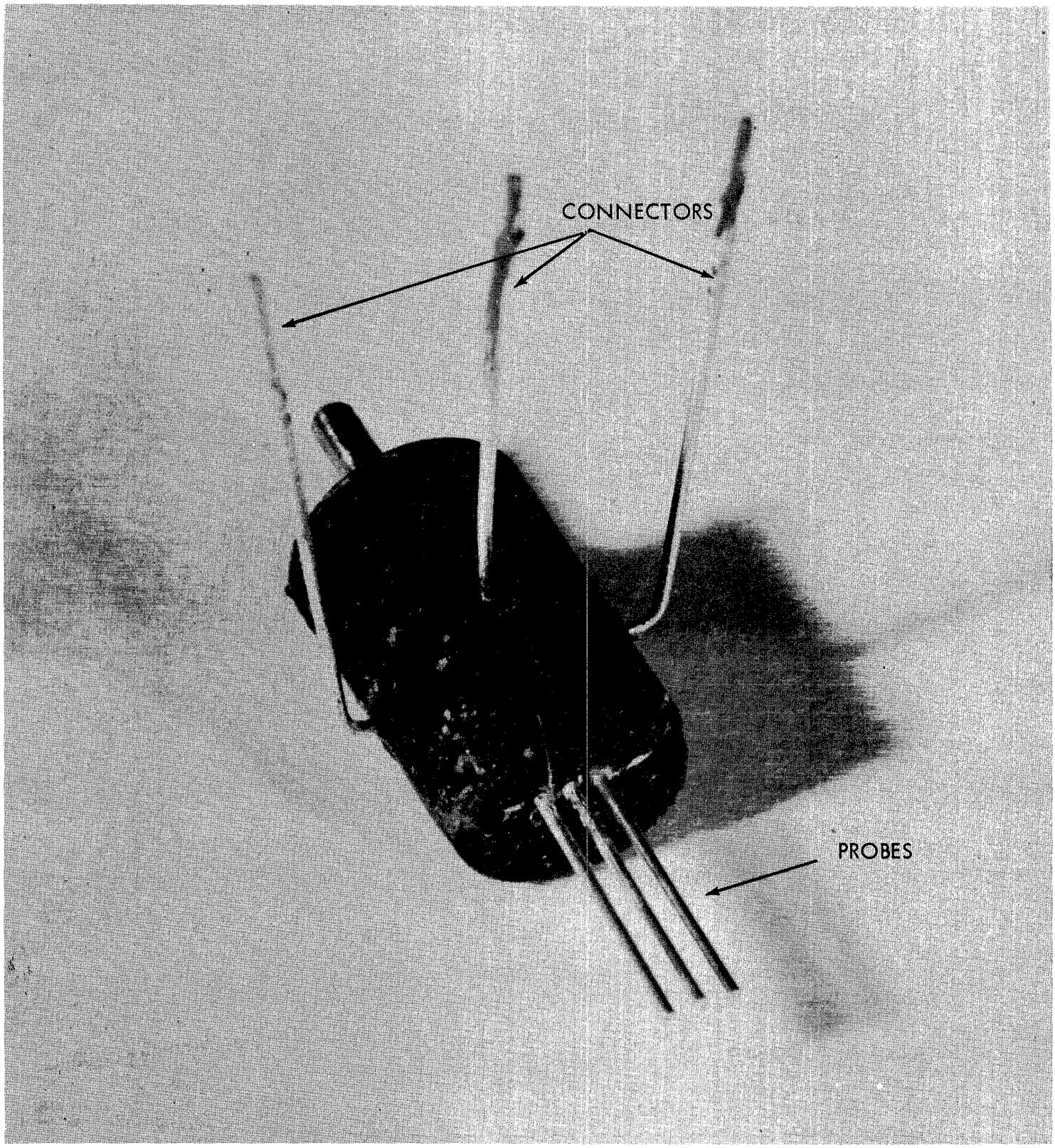


FIGURE 3 - 3-HOLE PROBE

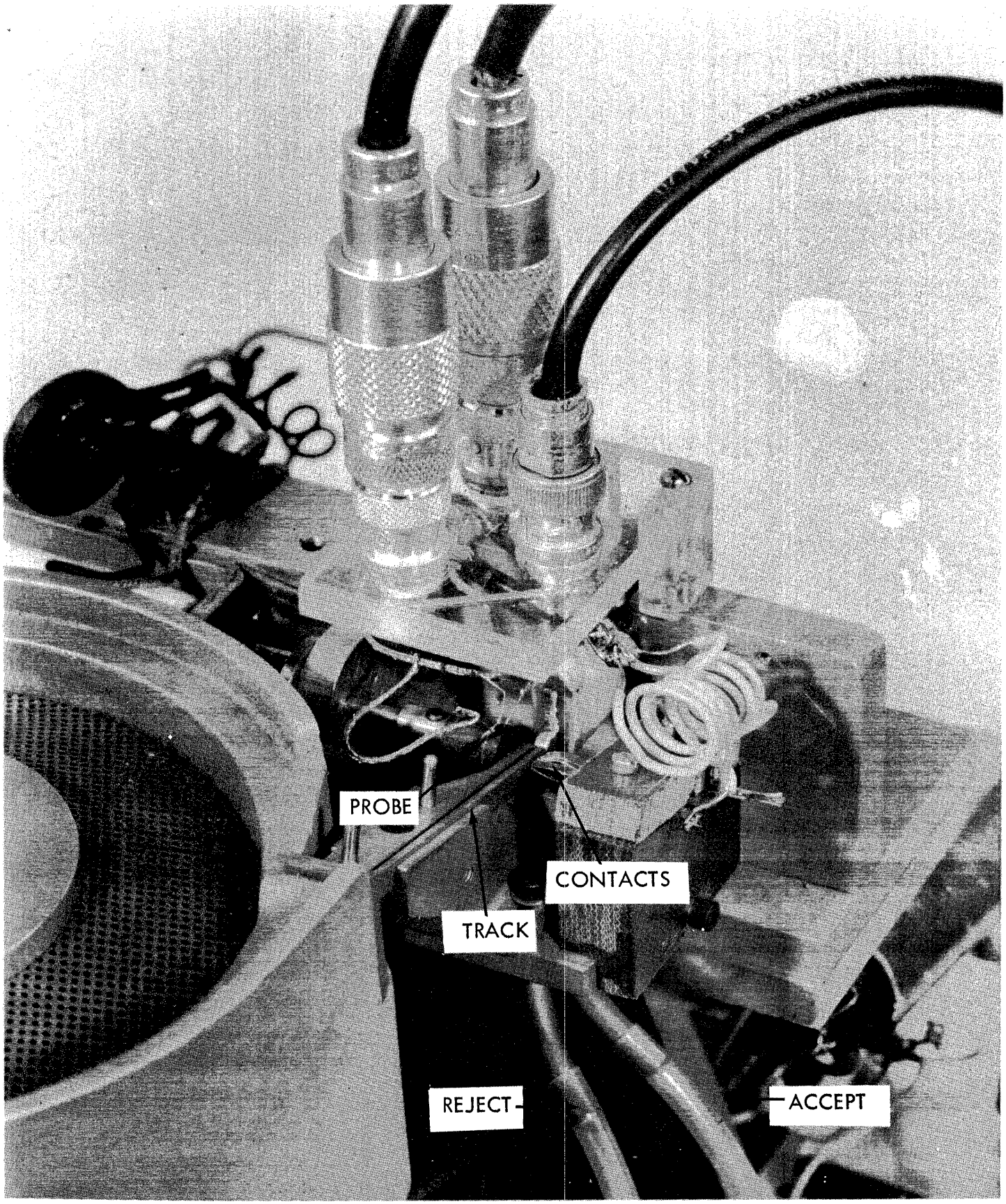


FIGURE 4 - 3-HOLE PROBE AND CONTACT ASSEMBLY

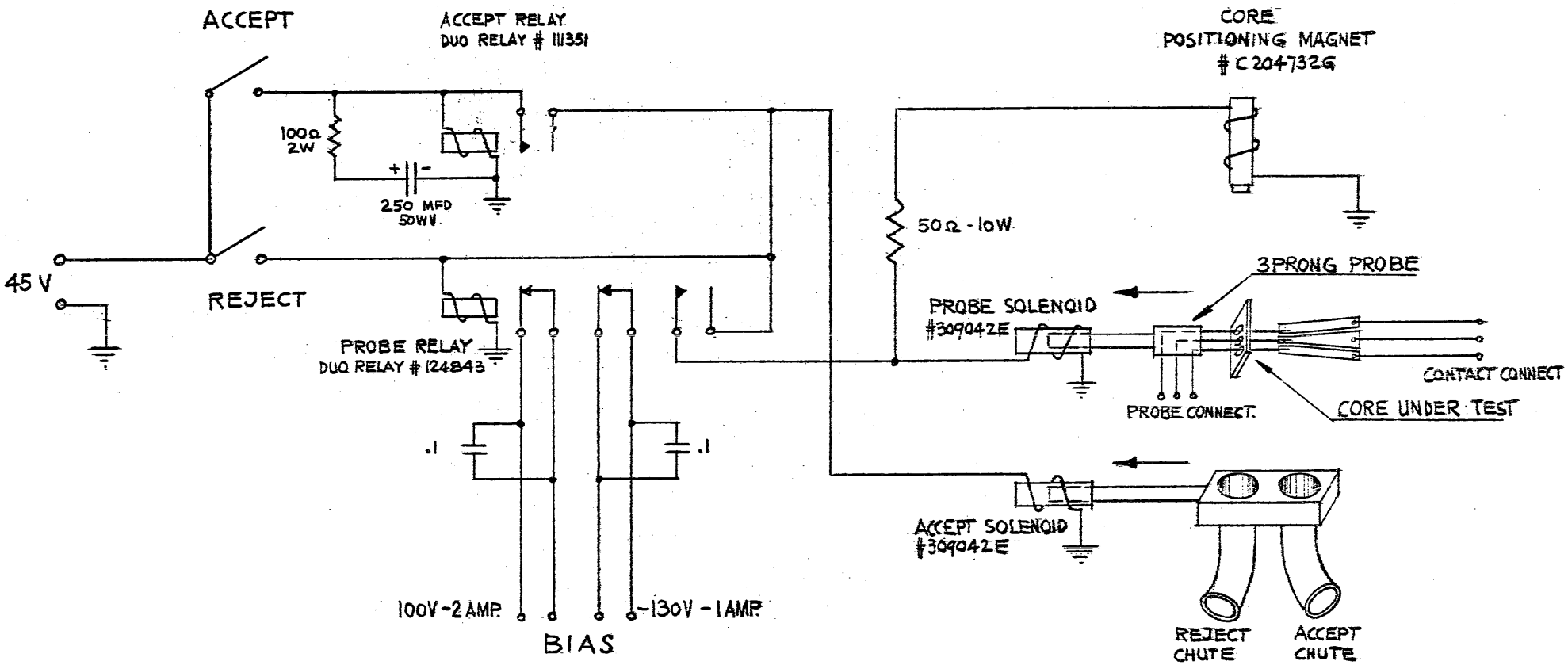


FIGURE 5 - MULTIPATH CORE HANDLER

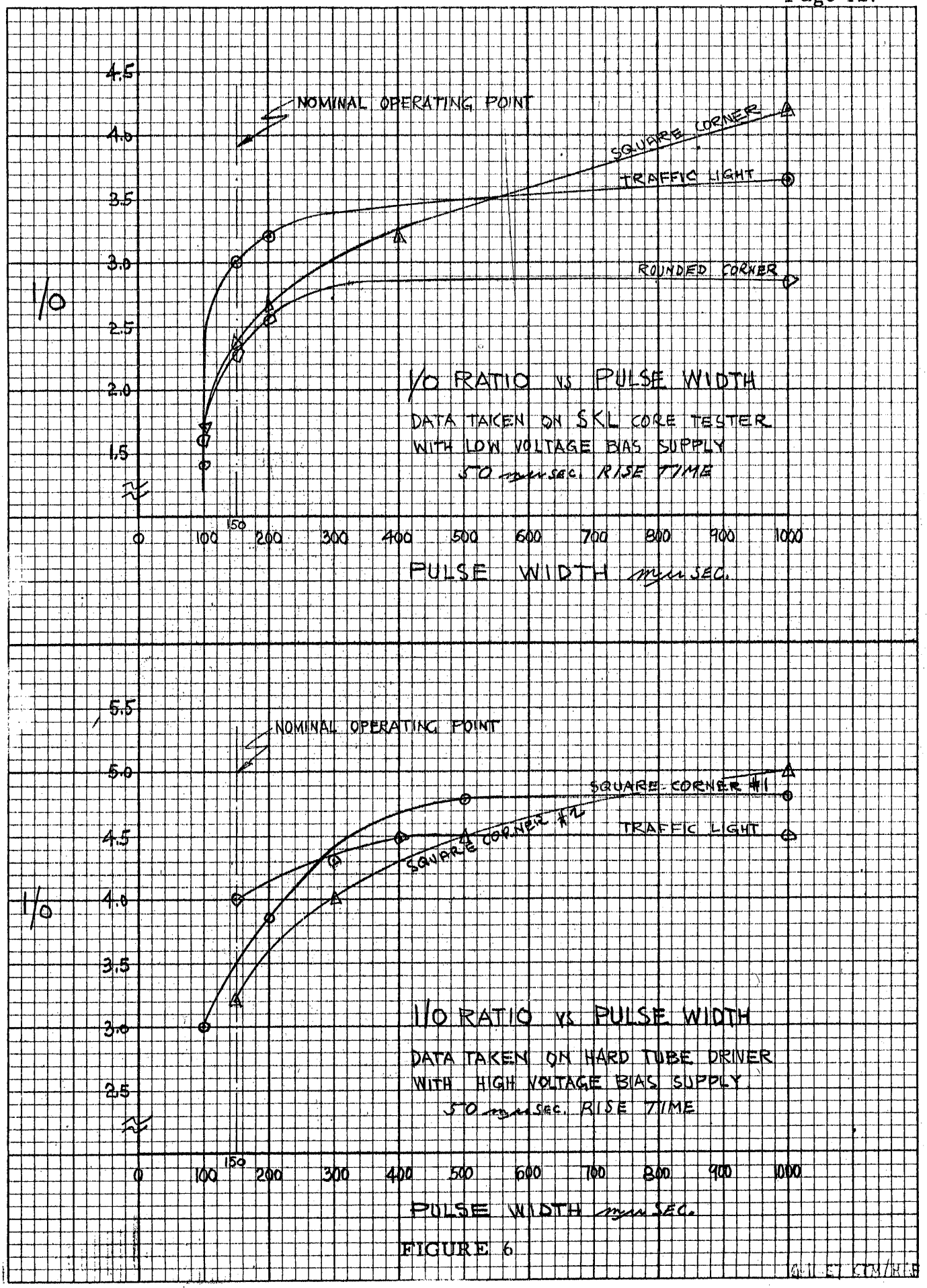

NOMINAL OPERATING POINT
SQUARE CORNER
TRAFFIC LIGHT
ROUNDED CORNER
1/0
1/0 RATIO vs PULSE WIDTH
DATA TAKEN ON SKL CORE TESTER
WITH LOW VOLTAGE BIAS SUPPLY
.50 μsec. RISE TIME
PULSE WIDTH μsec.
NOMINAL OPERATING POINT
SQUARE CORNER #1
SQUARE CORNER #2
TRAFFIC LIGHT
1/0
1/0 RATIO vs PULSE WIDTH
DATA TAKEN ON HARD TUBE DRIVER
WITH HIGH VOLTAGE BIAS SUPPLY
.50 μsec. RISE TIME
PULSE WIDTH μsec.

FIGURE 6

III. CORE TESTING EQUIPMENT

A. PULSE POWER AMPLIFIER: Designed by G. Constantine, Jr.

The pulse power amplifier is a set of six blocking oscillators to be used for pulse amplification and pulse shaping (see Figure 2A). The pulse power amplifier requires only 115 volts a.c. and 150 volts d.c. from external power supplies. Each input is a.c. coupled with a 3 μs time constant and an input resistance of 20 kilohms. Each output is d.c. coupled directly across a 220 ohm resistor. The circuit is shown in Figure 3A and a schematic of the service wiring in Figure 4A.

The amplitude of the required input trigger (at the grid of the trigger tube) as a function of pulse repetition rate is shown below in Figure 1A. Input triggers of less than rated amplitude will either cause consecutive output pulses to have different amplitudes or cause a complete absence of any output. The maximum pulse repetition rate is 2.5 megapulses/second.

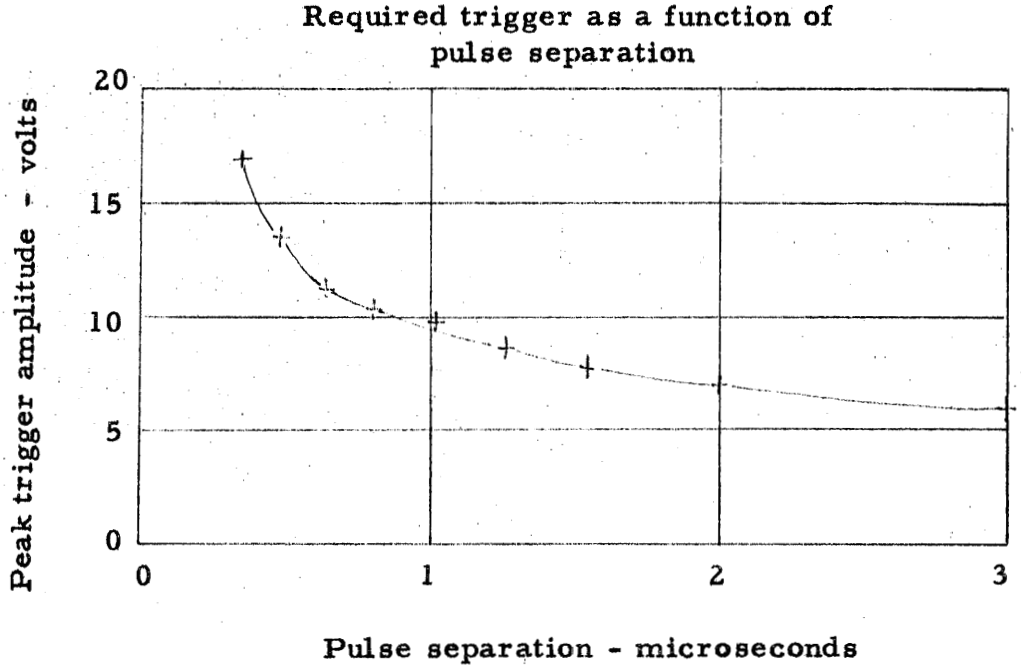


FIGURE 1A

III. A. (Continued)

The output of the blocking oscillators with a 30 μμf load:

40 volt minimum peak output voltage.
100 mμs maximum duration above 10% of peak output voltage.
80 mμs duration above 10 volts.
30 mμs minimum duration above 30 volts.
25 mμs rise time from 10% to 90% of peak amplitude.

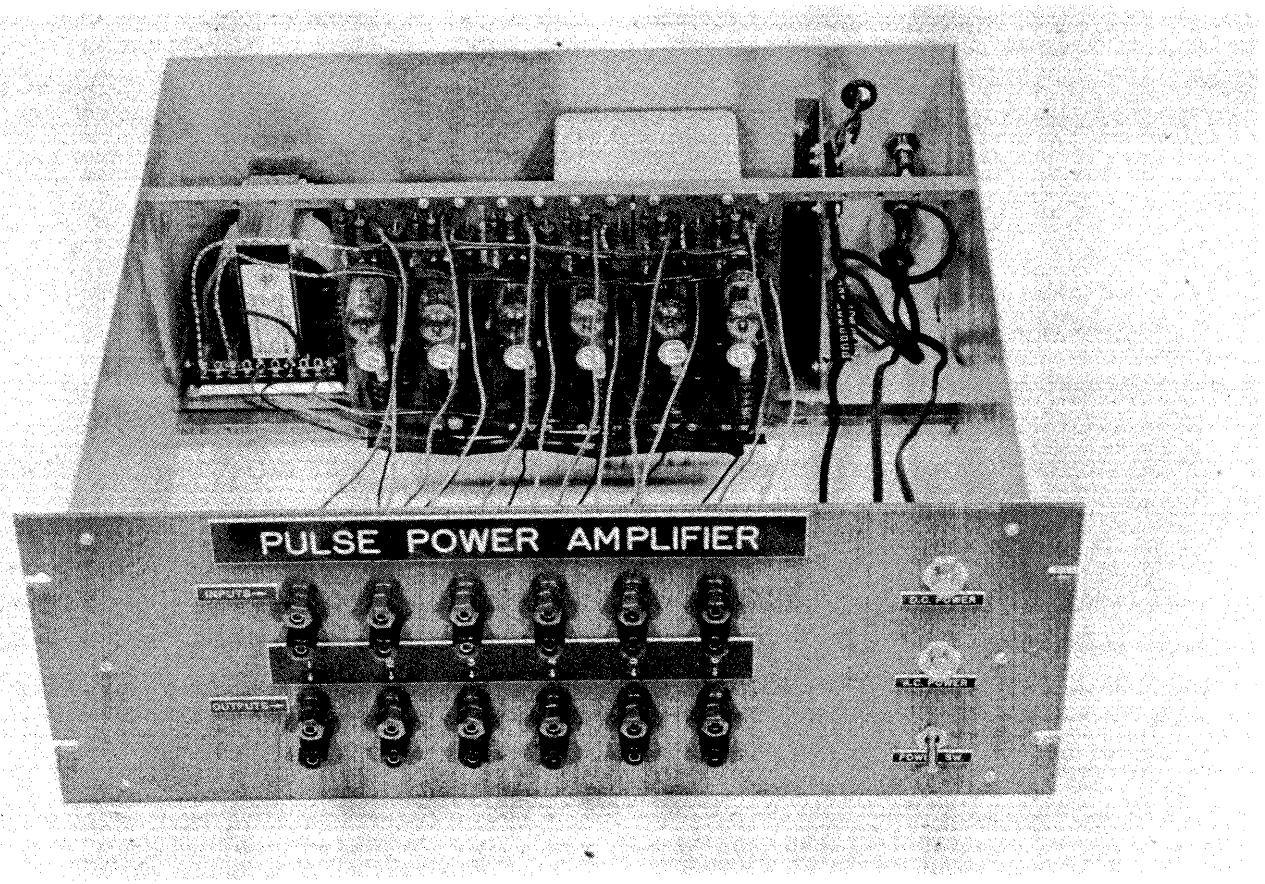
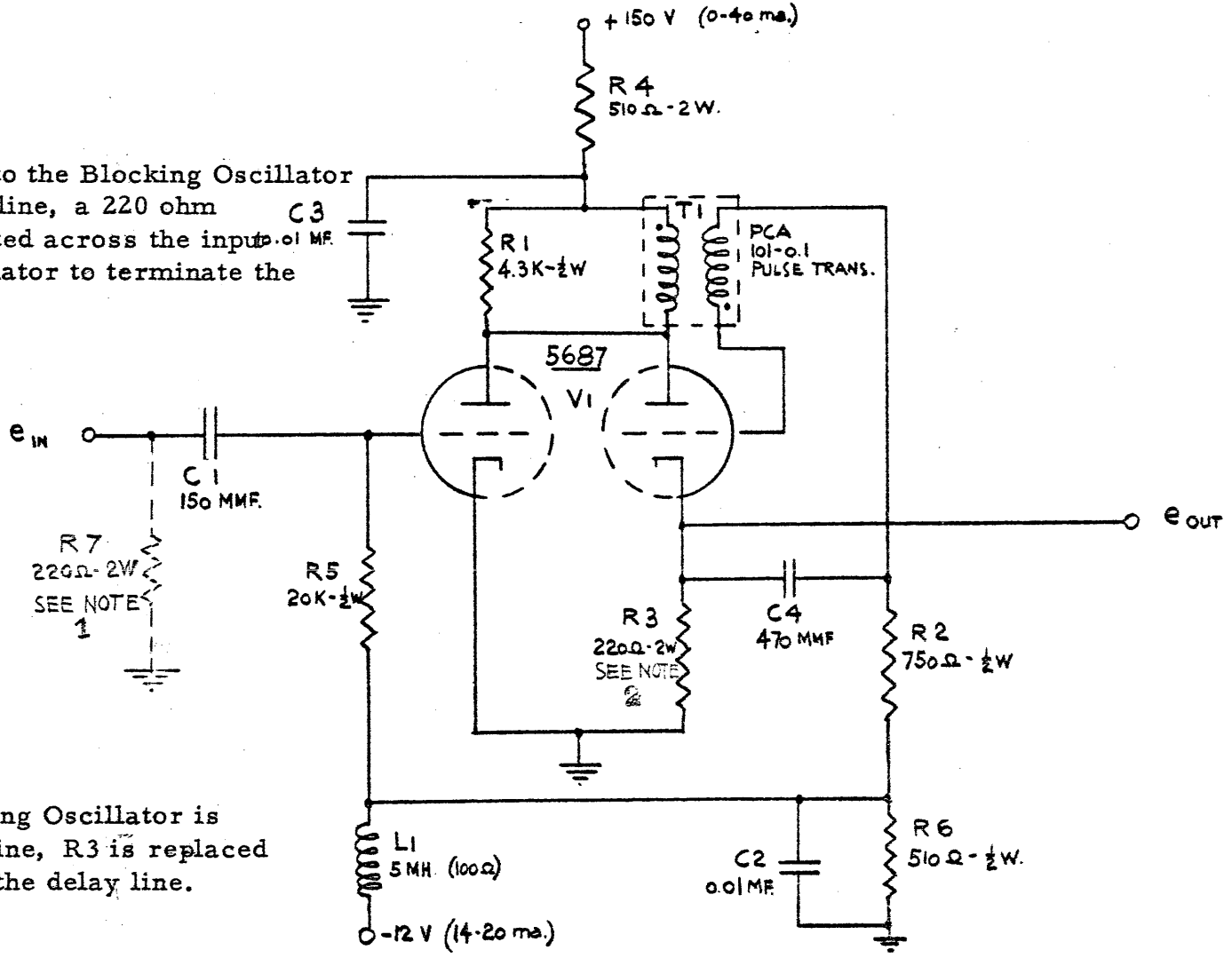


FIGURE 2A - PULSE POWER AMPLIFIER

Note 1: If the input to the Blocking Oscillator comes from a delay line, a 220 ohm resistor R7 is inserted across the input of the blocking oscillator to terminate the delay line.



Note 2: When Blocking Oscillator is followed by a delay line, R3 is replaced by Z_o (220 ohms) of the delay line.

FIGURE 3A - BLOCKING OSCILLATOR

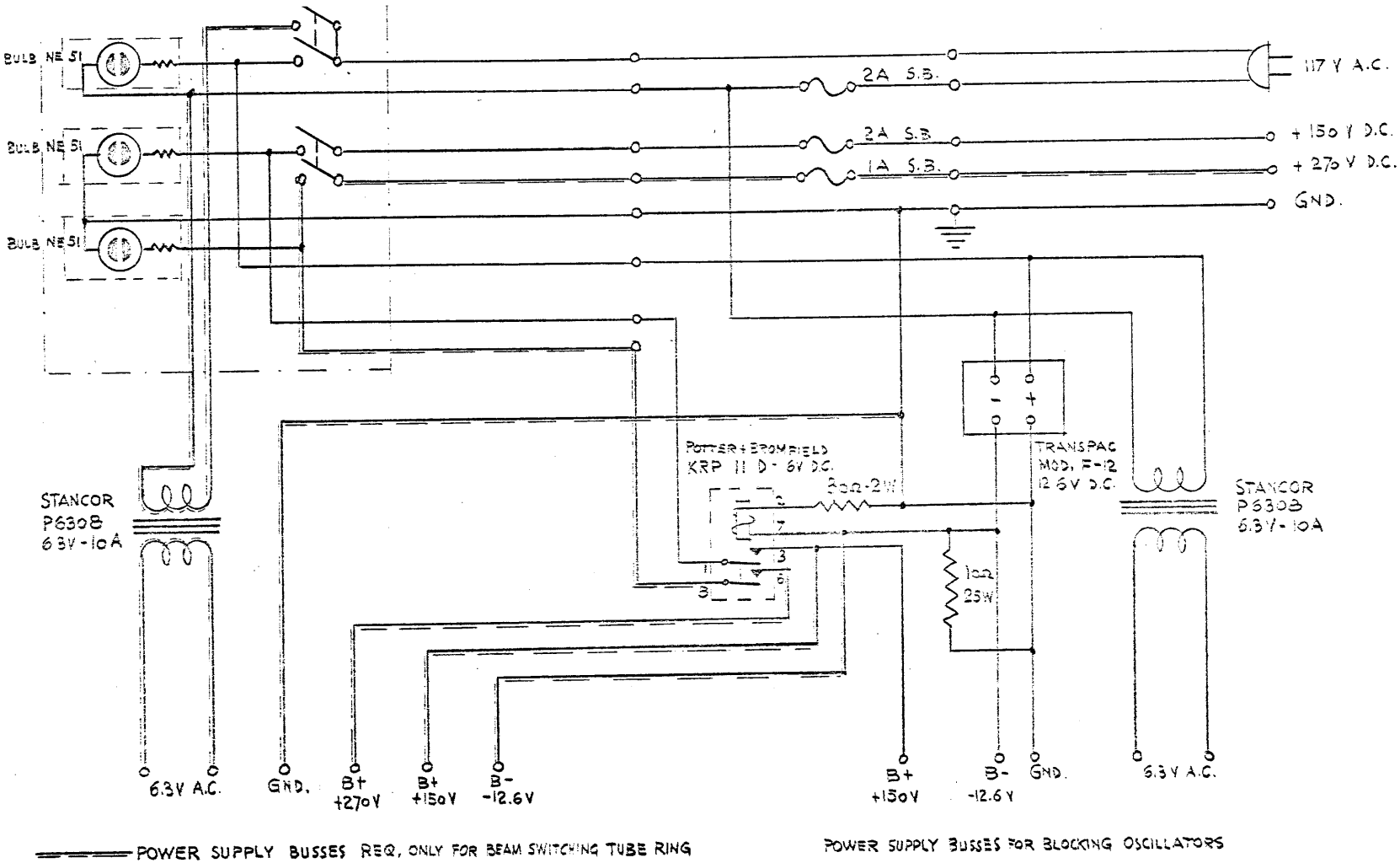


FIGURE 4A - POWER DISTRIBUTION CIRCUIT

III. B. DELAY LINE TIMING RING: Designed by G. Constantine, Jr.

The delay line timing ring provides a series of timing pulses to be used for programming a series of operations. A photograph of the unit is shown in Figure 1B and a block diagram of the system is shown in Figure 2B. An Electro-Pulse Model 3420B pulse generator is used for generating the pulses which set the basic repetition rate. Six delay lines (Shallcross #T-30129) provides the delay between consecutive pulses. Eight blocking oscillators provide the required narrow output pulses. The Electro-Pulse generator is a commercial product. The delay lines and blocking oscillators are custom built in a single unit (called the delay line unit).

1. Operation of Unit

The Electro-Pulse generator establishes the basic timing cycle duration. This generator produces odd and even timing pulses, their pulse repetition frequency being established by the multivibrator clock of the Electro-Pulse unit. The time interval between pulse outputs of the delay line timing ring is accomplished by varying the length of the individual groups of lines.

Several variations of the intended mode of operation are feasible. For example, input #1 of the delay line unit may be driven by a square wave generator. Input #2 may be connected to output #4. Then, output #4 and output #5 will be separated only by the 20 mμs delay inherent in each blocking oscillator. The set of timing pulses may then be spread over about 6 μs with an independently variable repetition rate. This type of operation would allow the observation on an oscilloscope of an entire pulse testing pattern in spite of a low repetition rate.

2. Operating Characteristics

a. Repetition Frequency Range

III. B. 2. a. (Continued)

1. The upper limit is

a. 2 Mc with no delay line set at 0.6 μs or longer
b. 1.5 Mc with no restriction on the available delay line settings

2. The lower limit is set by the lower frequency limit of the Electro-Pulse generator

b. Timing Pattern Restrictions

The spacing between consecutive pulse outputs is variable in steps of 0.02 μs from 0.02 μs to 1.02 μs. Therefore, the pulses may be set in any pattern for timing cycle durations of 1 μs or less. Timing cycles as long as 8 μs may be obtained if the pulse outputs may have equal separations.

c. Output Signal Characteristics

The output of the unit will be determined by the performance characteristics of the blocking oscillators. See section on Pulse Power Amplifiers.

d. Spurious Output Signals

Reflections in the delay lines may add up to as much as 20 volts peak in a pulse about 0.1 μs after the main output pulse. Subsequent spurious pulses are lower in amplitude. The 0.02 and 0.04 μs delay line sections seem to cause the worst reflections. Crosstalk between delay lines is visible on an oscilloscope, but is generally of negligible amplitude.

3. Design

The output pulses are furnished by a set of blocking oscillators (see section III-A on Pulse Power Amplifier). The time be-

III. B. 3. (Continued)

tween consecutive outputs is obtained by using a delay line to delay the first blocking oscillator output to provide the input to the second blocking oscillator. Where a blocking oscillator is followed by a delay line, the cathode resistor of the blocking oscillator is replaced by the characteristic impedance (220 ohms) of the delay line. If the input to a blocking oscillator comes from a delay line, a 220 ohms resistor is connected across the input of the blocking oscillator to terminate the delay line. This is done internally on the blocking oscillator printed circuit cards.

The set of delay lines and the front panel on which they are mounted was constructed especially for the delay line timing ring by Shallcross Manufacturing Company. The delay line set is Shallcross #T-30129.

A schematic of the service wiring is identical to that of the Pulse Power Amplifier.

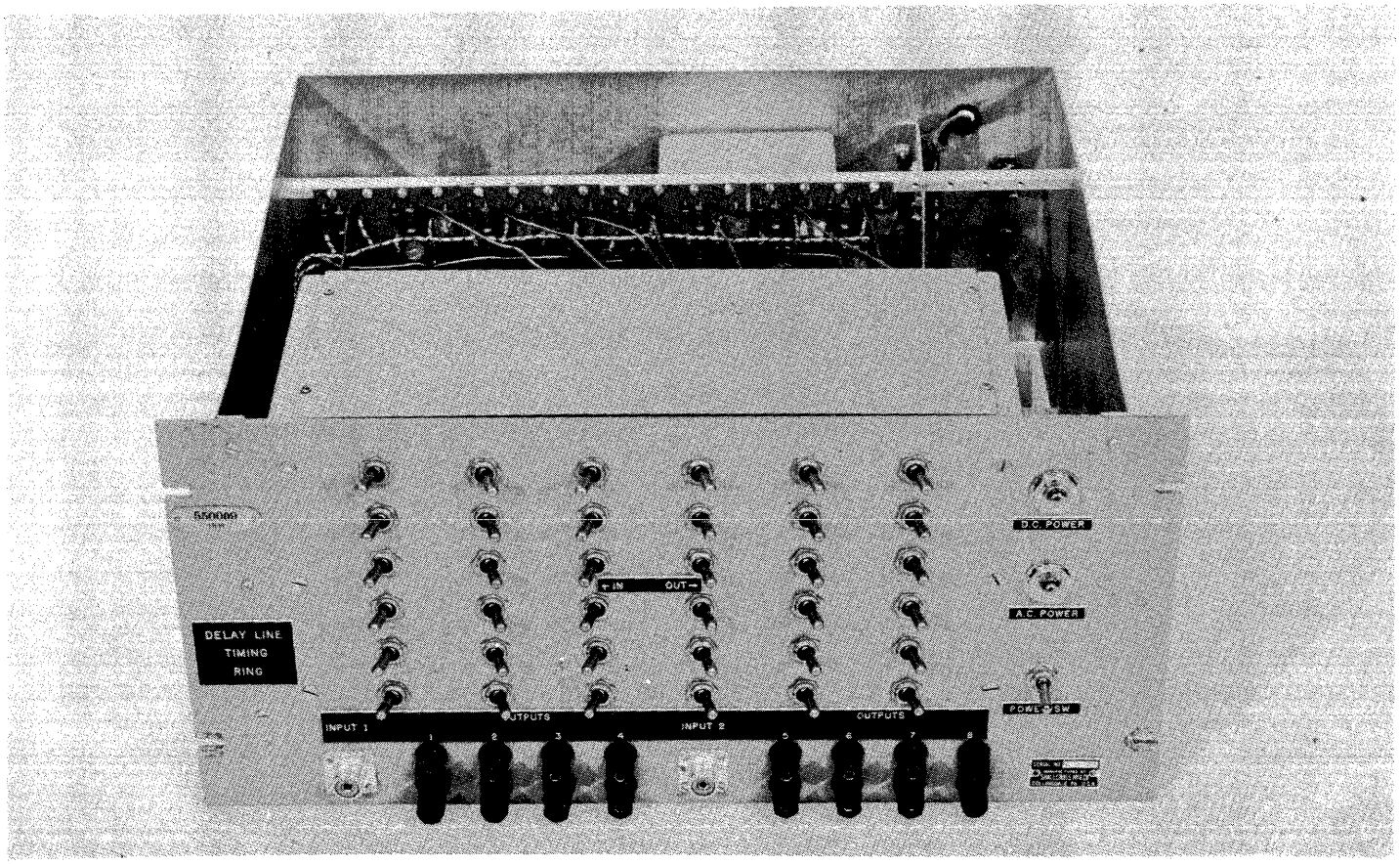
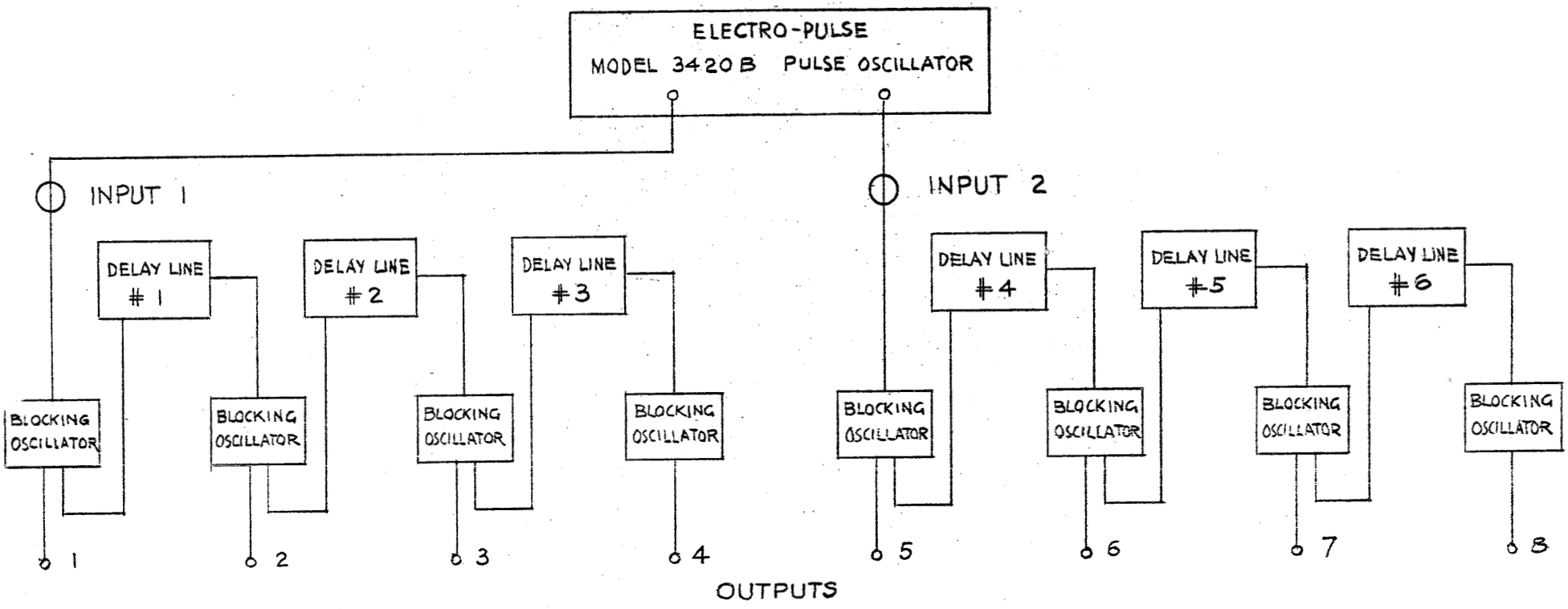


FIGURE 1 B - DELAY LINE TIMING RING



DELAY LINES: SHALLCROSS DELAY LINE
UNIT # T-30129

FIGURE 2B - BLOCK DIAGRAM OF DELAY LINE TIMING RING

III. C. MBST HIGH-SPEED TIMING RING:

Designed by R. R. Booth and R. J. Yeager

The Magnetron Beam Switching Tube (MBST) high-speed timing ring is a switching device with ten outputs. A signal can pulse ten consecutive targets with a range of 4 μs to 0.5 μs in a free-running state, giving a pulse repetition rate of 0.250 Mc to 2.0 Mc for each output. The units must be driven externally for channel frequencies less than 250 Kc.

The unit has two primary parts.

(1) The MBST and associated amplifiers mounted on a chassis behind the front panel (see Figure 1C).

(2) The power supply and blocking oscillators at the rear of the unit. These are identical to the units described in section III-A on the Pulse Power Amplifier.

1. Front Section - Figure 1C

The front section contains a Haydu M0-10-R MBS Tube and twelve 6CL6's used as amplifiers. Ten are located at the rear of the chassis and supply the amplified target signal to the blocking oscillators. These are called target amplifiers. The remaining two are grid amplifiers and are used to amplify signals from an Electro-Pulse #3420B Pulse Generator. The outputs from these two amplifiers switch the Haydu MBS Tube. A schematic of the unit is shown in Figure 2C.

a. Grid Amplifier Characteristics

Tube: 6CL6
Plate Voltage: +270 volts
Screen Voltage: +150 volts
Bias: +12 volts
Amplification: 5
Grid Signal from Electro-Pulse: +40 volts
MBS Tube Grid Signal: +200 volts

III. C. 1. b. Target Amplifier Characteristics

Tube: 6CL6
Plate Voltage: +270 volts
Screen Voltage: +150 volts
Bias: -2
Amplification: 14
Grid Signal to Amplifier: -10 volts
Amplifier Output: +140 volts

c. MBS Tubes Characteristics

Tube: Haydu M0-10-R
Target Voltage: +150 volts to 0 volts
Spade Voltage: +105 volts to 270 volts
Grid Signal: -200 volts to -60 volts
Grid Bias: +18 volts
See Electronics, April 1956, page 122

d. The MBS Tube has two modes of operation: driven and free-running

1. Driven: The MBS Tubes may be driven by an outside source of suitable magnitude. (Electro-Pulse #3420B) It will give frequencies of up to 250 Kc. Target voltage: +150 volts. Spade voltage varies with MBS Tubes. (See paragraph below on calibration.)

2. Free-Running: The MBS Tubes will free-run when spade voltage reaches about +125 volts, regardless of grid signal. The frequency may be increased further by decreasing target voltage. It is most important that the tube be adequately cooled in this mode of operation.

e. Calibration for Driven Operation

In normal operation the repetition rate for one output of the MBS Tube should be 1/5 that of the Electro-Pulse. If the spade voltage is raised, this ratio can be made 1/4, 1/3, or 1/2. A good calibration procedure is as follows.

III. C. 1. e. (Continued)

The Electro-Pulse is set to 10 μs between pulses. Set spade voltage control on front panel to position 1. Then the calibration potentiometer on the rear of the chassis is adjusted until the MBS Tube has a 50 μs repetition rate as seen on any one of the target outputs with an oscilloscope. For proper operation the spade voltage should now be at 105-115 volts.

2. Back Section

The back section contains a set of blocking oscillators to be used for pulse amplification and for pulse shaping. This unit is ready to operate if it is connected to 115 volts a. c. and to 150 volts d. c. and if the power switches are "on." The input to a blocking oscillator is connected directly (or through a diode logic board) to the output from the desired target amplifier. The output of the blocking oscillator is connected to the input terminals of a current driver. The blocking oscillator characteristics are shown in section III-A on the Pulse Power Amplifier. A schematic of the circuit between the external power sources and the supply busses to the blocking oscillators is shown in Figure 2C.

Where low frequency operation is being used for all laboratory experiments, a simple free-running multivibrator may be used to replace the Electro-Pulse 3420B Generator. A circuit for a 10 Kc unit is shown in Figure 3C.

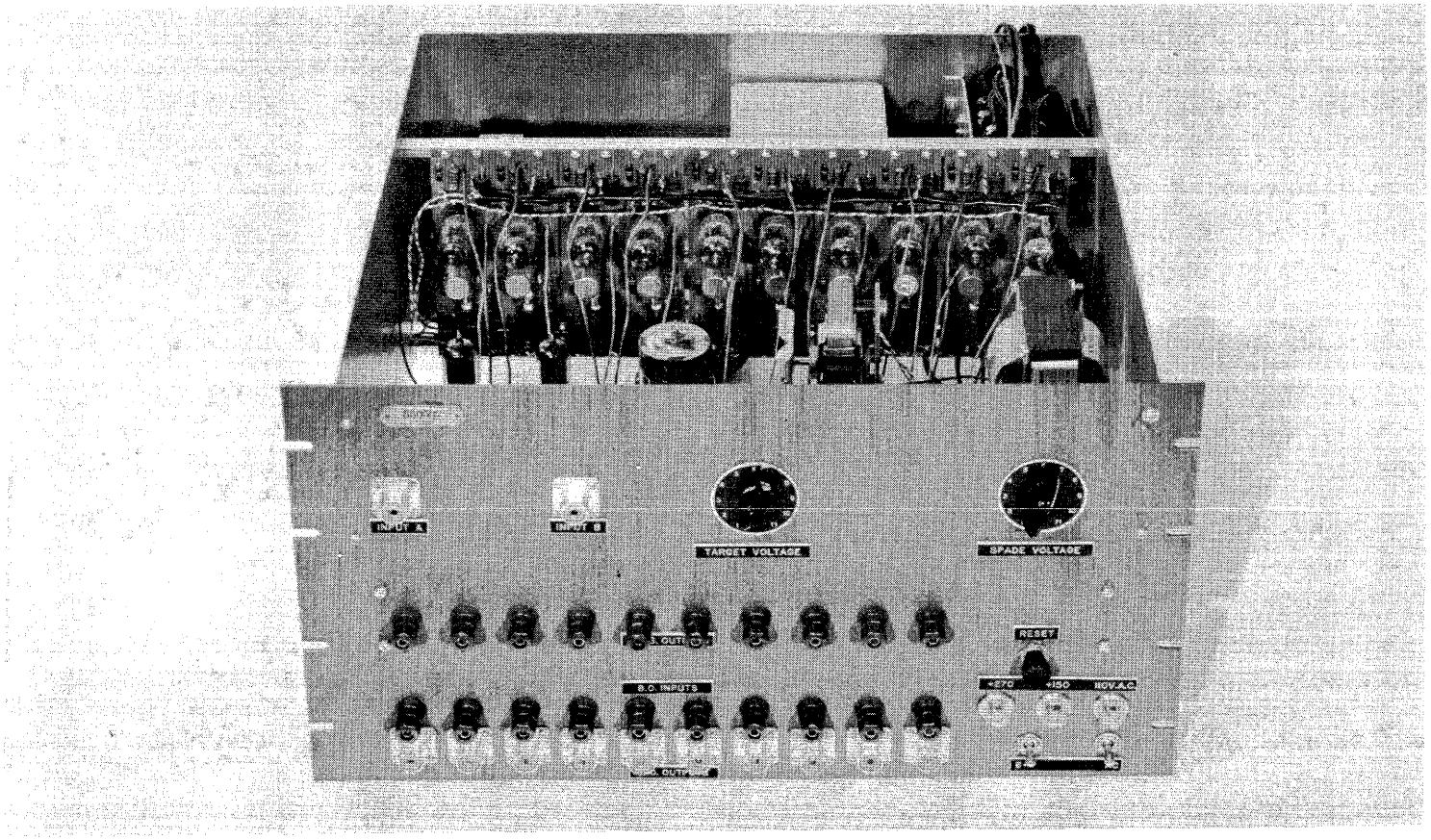


FIGURE 1C - MBST HIGH SPEED TIMING RING

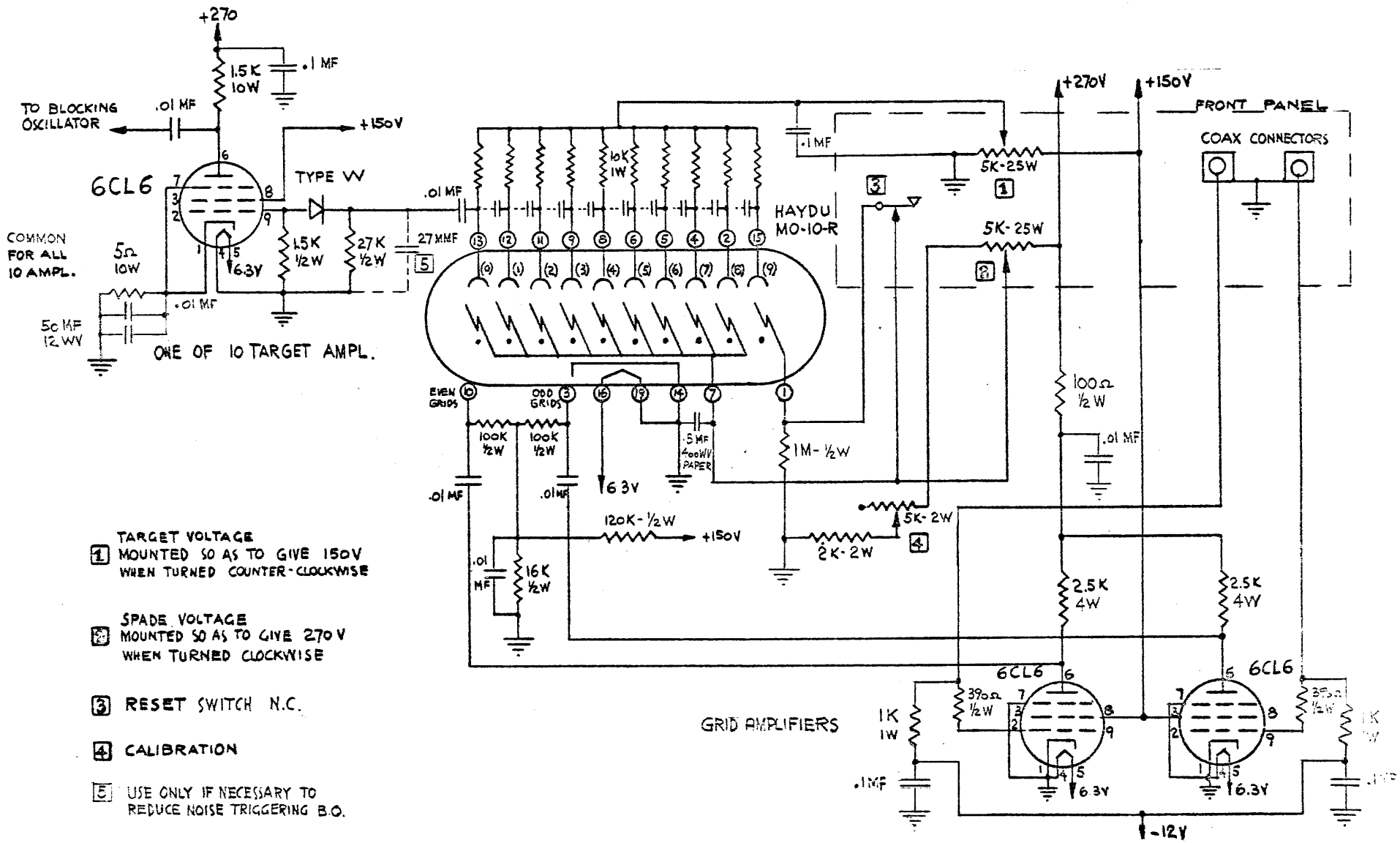


FIGURE 2C - TIMING RING

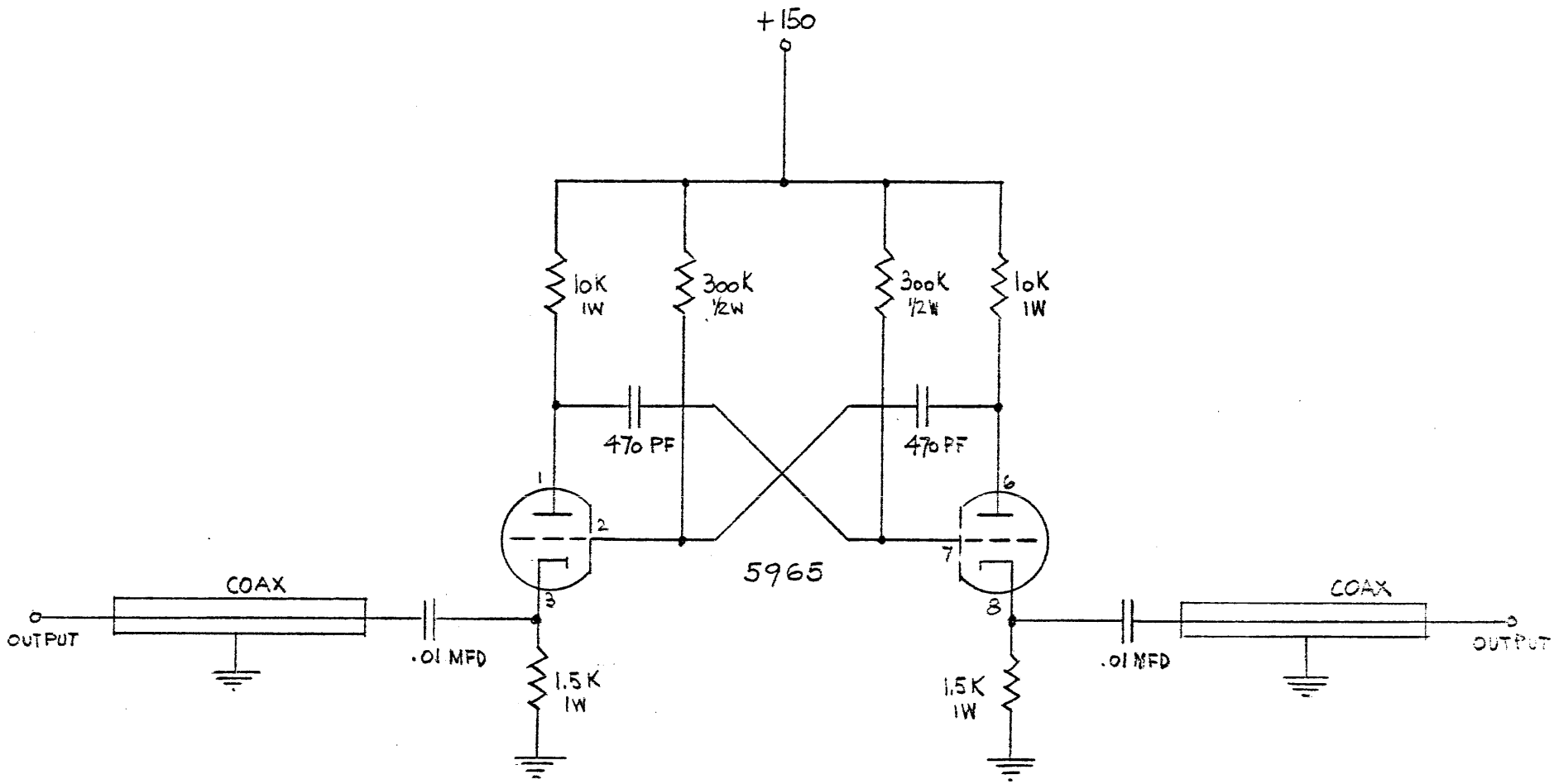


FIGURE 3C - 10 KC MULTIVIBRATOR

III. D. DRIVER LOGIC UNIT: Designed by N. C. Ford

This unit was designed primarily to furnish pulse logic to the fast rise drivers described in section III-F. The correct pulse pattern is accomplished by means of lever switches contained on the front panel of the unit (see Figure 1D). Each vertical pair of switches represents a different timing point of a ten point ring (see Figure 2D). By locating the switches in their proper position, any combination of read and write full-select pulses, and read, write and inhibit half-select pulses can be obtained. The circuitry is such that when any of the upper switches are in the "Z" inhibit position, an output also occurs from the "W" write channel. This allows the duplication of a memory cycle in the writing of a zero into a multipath core structure.

When any of the lower bank of 10 switches is energized, their channels will produce n disturb signals as determined by the position of the 2^n selector switch. There is no restriction on any of two vertical switch positions. Necessary time delays are incorporated into the unit so that the disturb pulses on the lower switch will come after the full-select pulse that had been set on the upper switch. In effect, the unit is a 10 stage ring which can be expanded up to 20 points depending on the number of disturb channels used.

The circuitry of the unit is shown in Figures 2D, 3D, and 4D. The multivibrator clock drives the grids of the Haydu Beam Switching Tube directly when normal full-select outputs are desired. However, when half-select disturb outputs are wanted, the output from the 1/2 select amplifiers (#3, 4, and 6) causes the modified trigger TR-1 to turn off and to block the flow of clock pulses to the beam switching grids. This trigger will not reset until the clock pulses follow down the scale-of-two counters (the 6 triggers labeled TR-3). The number of disturb pulses is determined by the setting of the 2^n selector switch. In this unit, a maximum of 128 disturb pulses can be obtained from each disturb channel switch setting.

The outputs of this unit are obtained from the cathode followers. The positive going signal is in excess of 100 volts in amplitude. The unit may be modified by the use of blocking oscillators in the output stages to allow driving the two channel current drivers. By using suitable power amplifiers in the output stages to drive mercury relay-condenser discharge drivers, this logic unit can replace the cumbersome cam rack logic presently used for manual and semi-automatic testing of toroids.

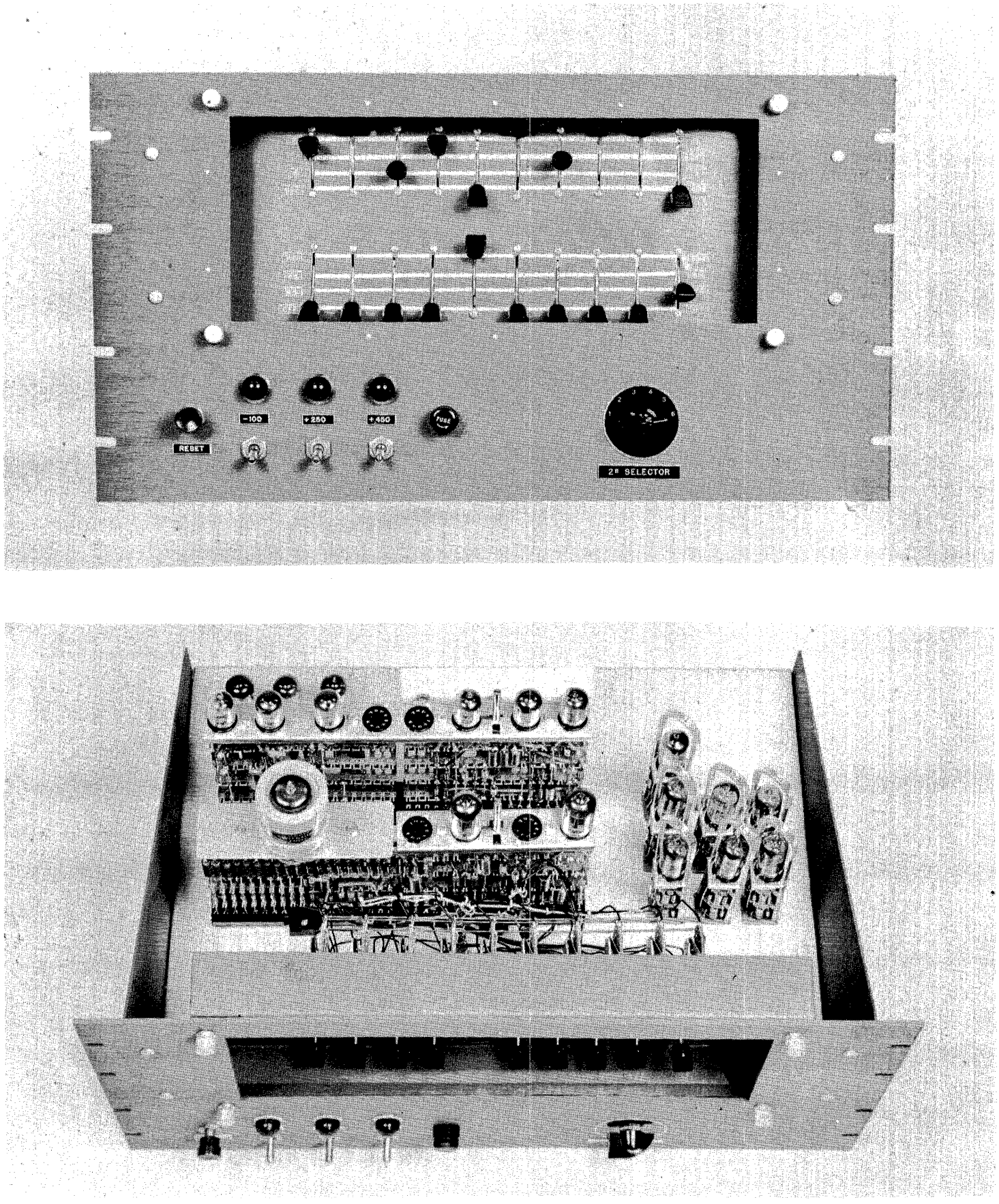


FIGURE 1 D - DRIVER LOGIC UNIT

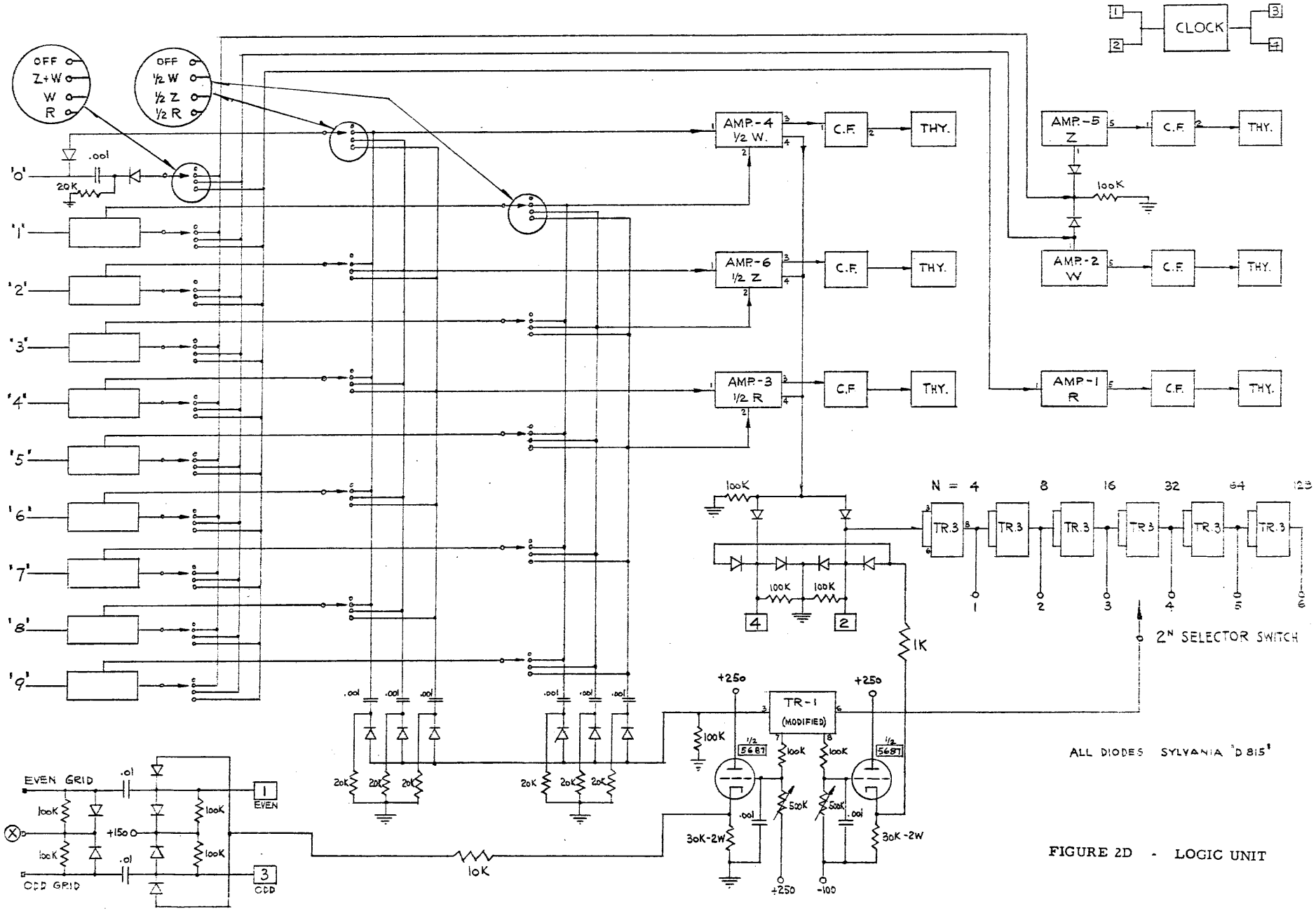


FIGURE 2D - LOGIC UNIT

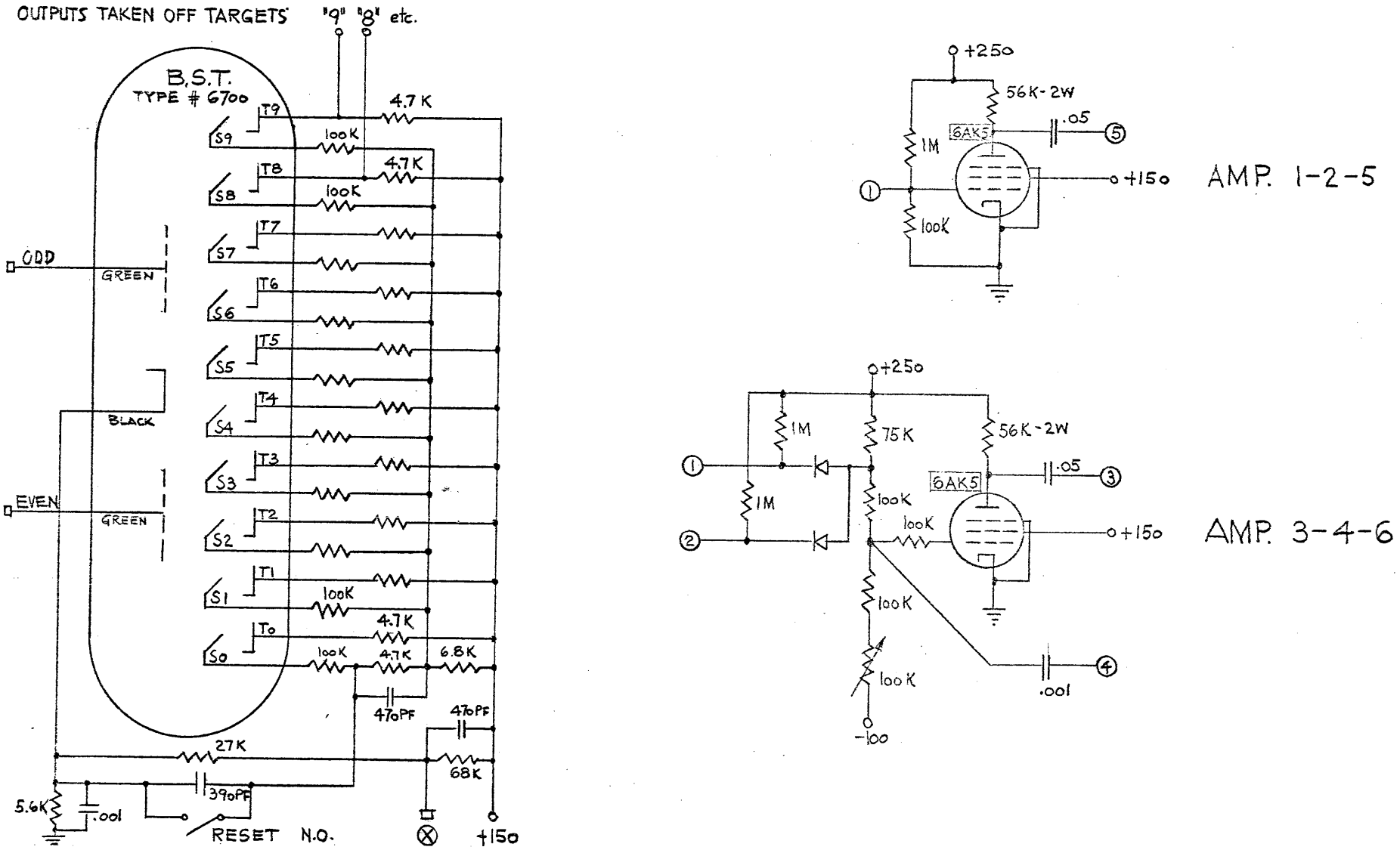


FIGURE 3D - LOGIC UNIT DETAILS

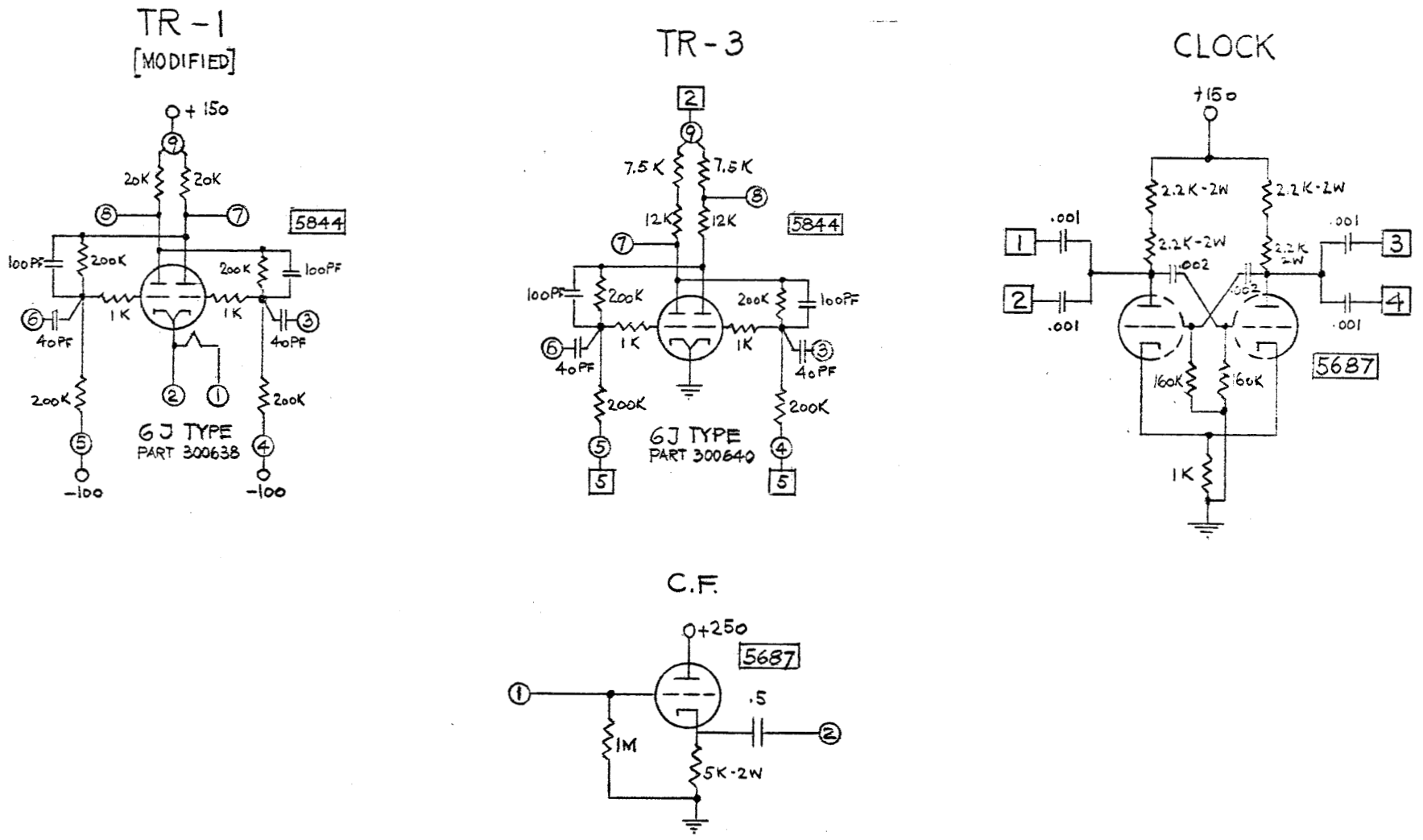


FIGURE 4D - LOGIC UNIT DETAILS

III. E. MODIFIED SPENCER-KENNEDY LABORATORIES #503 PULSE GENERATOR CORE TESTER: Designed by J. J. Mackson

1. Operation of Core Tester

This core tester is a piece of test equipment which allows the operator to set up a complex core testing program to test a ferrite core. This equipment will allow one to get as many as 9 read or write full-select pulses in succession, or various combinations of these pulses. The core tester consists of three parts: Part A, Core Tester Logic Circuits; Part B, Relays and their Driving Circuits; and Part C, Modified Spencer Kennedy Fast Rise Pulse Generator. The tester logic unit and associated relays are shown in the photograph in Figure 1E.

a. Part A - Core Tester Logic Circuits

The function of the logic circuits is to give the operator a desired program. This is done by using 5 "and" circuits in conjunction with a multivibrator, binary counter, flip-flop, and a MBST (Haydu Type (MO-10) 6700). (See Figures 2E and 3E.)

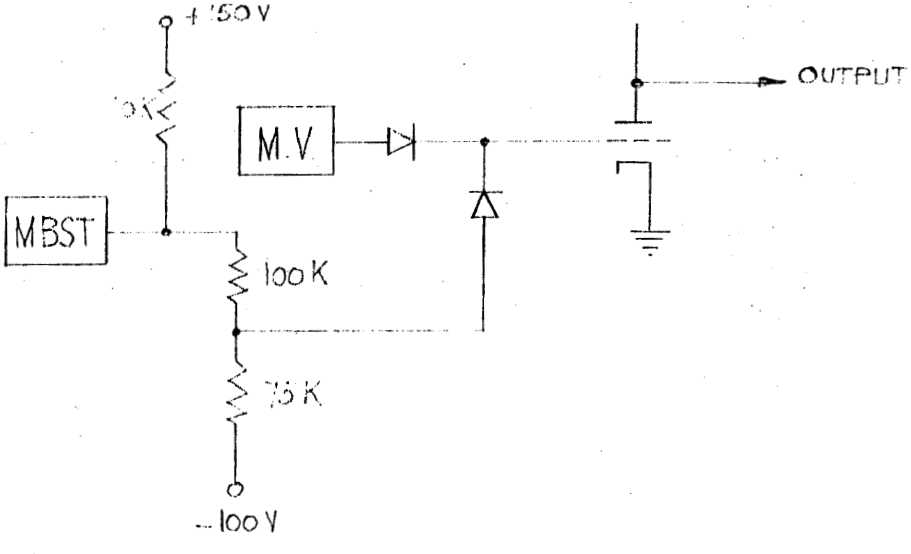
Each "and" gate is given a different job. If "and" gates 1 or 2 are open, a half-select read or half-select write output will be given respectively. "And" gates 3 or 4 will give a full-select read or full-select write output respectively. "And" gate 5 is used to give a delay between program pulses, and is therefore called "and" off select gate. The opening and closing of these gates is dependent on the MBST whose operation is dependent upon the flip-flop.

A multivibrator, free-running at 50 cps, was used as a pulse source. The output of the multivibrator was taken off the cathode because it gave a sharp positive going pulse which when going through the "and" gate and amplified would give a sharp negative-going spike which is necessary to change the state of the triggers of the counter and the flip-flop.

III. E. 1. a. (Continued)

The MBST has 10 outputs. Each one of these outputs is connected to ten 5-position switches. The 5 outputs of the 10 switches are connected to one of 5 "and" gates, thereby making it possible to open any one of the "and" gates from 1 to 10 MBST outputs by simply turning 1 to 10 of the switches to position D+ for gate 1 or D- for gate 2 and etc. The output from the MBST is a negative-going pulse (see Figure 4E).

The "and" gate operates in this manner. The output of the multivibrator swings from -8.5 to 0.5 volts. The output of the MBST into the "and" gate is either a volt or two above ground or more negative than -8.5. It is seen from the diagram below that a signal will only get onto the grid of the amplifier when the MBST output is down. Since the MBST operates the "and" gates, no two gates can be opened at the same time.



Consider the operation of the logic circuits as a whole. Multivibrator pulses are waiting to get through the 5 "and" gates. An output of the MBST is fed to an "and" gate. The gate is opened. The multivibrator pulses are fed to the grid of its respective amplifier. The signal

III. E. 1. a. (Continued)

is inverted and amplified. For "gates" 1 or 2 this signal is passed through the counter to the flip-flop, which advances the beam of the MBST to another target. For "gates" 3, 4, or 5 the amplified signal goes directly to the flip-flop, which changes the state of the MBST. To summarize, a MBST output falls, this opens a gate. A negatively going pulse is fed onto the grid of the amplifier. The output of the amplifier is positively going. When the grid input swings positively, the amplifier falls negatively which changes the state of the flip-flop, which advances the MBST beam to another target which closes the gate. This cycle keeps repeating. Always be sure to push the reset button to start operation of logic circuits.

b. Part B - Relays and Their Driving Circuits

The output of the 4 amplifiers, signifying full read, full write, 1/2 read, and 1/2 write are fed to their respective relay driving circuits (see Figure 5E).

Their outputs are connected in series and its output is brought to the front panel and labeled trigger output. Two power supplies are used to give the correct amplitude of pulse desired for full-select and half-select pulses. The power that accompanies each full-select and half-select pulse is brought to the front of the panel and labeled power output. Because relays are used, a voltage power output will result and be of such polarity and magnitude as is assigned to one of the four driving circuits when it gives an output. Therefore, for every trigger output there will be a corresponding power output.

c. Part C - Modified Spencer-Kennedy Fast Rise Pulse Generator (SKFRPG)

The SKFRPG terminated in 51 ohms is used to switch the core which is to be tested. Its operation is as follows: The two coax jacks on the front panel of the core tester labeled trigger output and power output are connected to the trigger input, and the modification jack labeled on the

III. E. 1. c. (Continued)

SKFRPG (see Figure 6E). This modification allows one to obtain a larger range of voltage swings for your output pulse, which is determined by the two power supplies labeled full-select and half-select power. Because the trigger and power outputs are initiated in the SKFRPG at the same time, the delay line will charge up with a given voltage and polarity when the trigger is on. When the trigger turns off, the line will discharge. The amplitude and polarity of the output pulse is determined by the power output. The pulse width is determined by the delay line used. The repetition rate can be varied from 25 cps to 150 cps. The repetition rate is slow because a relay is used to charge and discharge the line.

A description of a pad to increase the rise time of the SKL generator can be found in Figure 3F in the section on the Fast Rise Time Thyratron Driver.

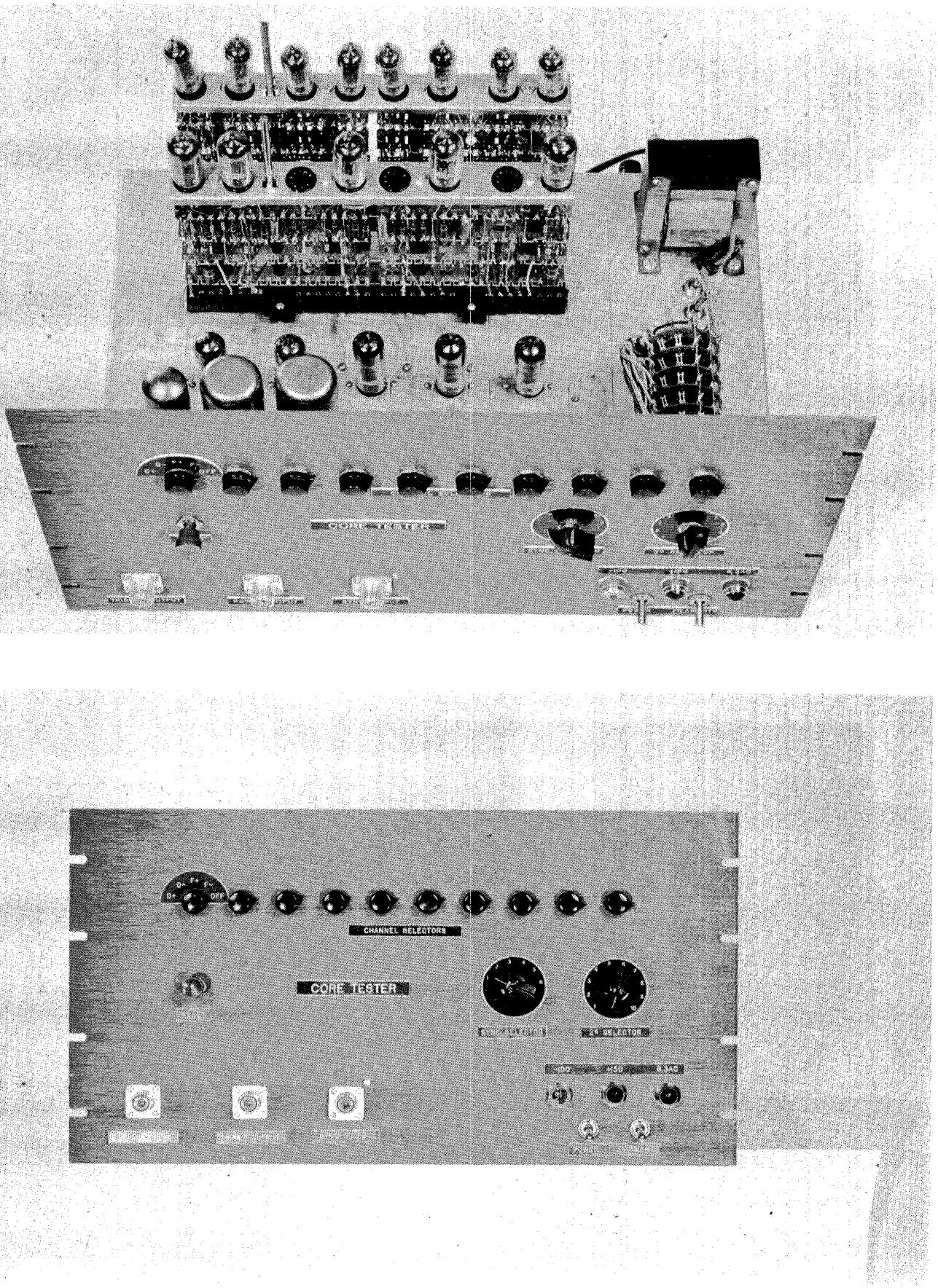


FIGURE 1 E - LOGIC PROGRAMMER FOR MODIFIED SKL #503 PULSE GENERATOR

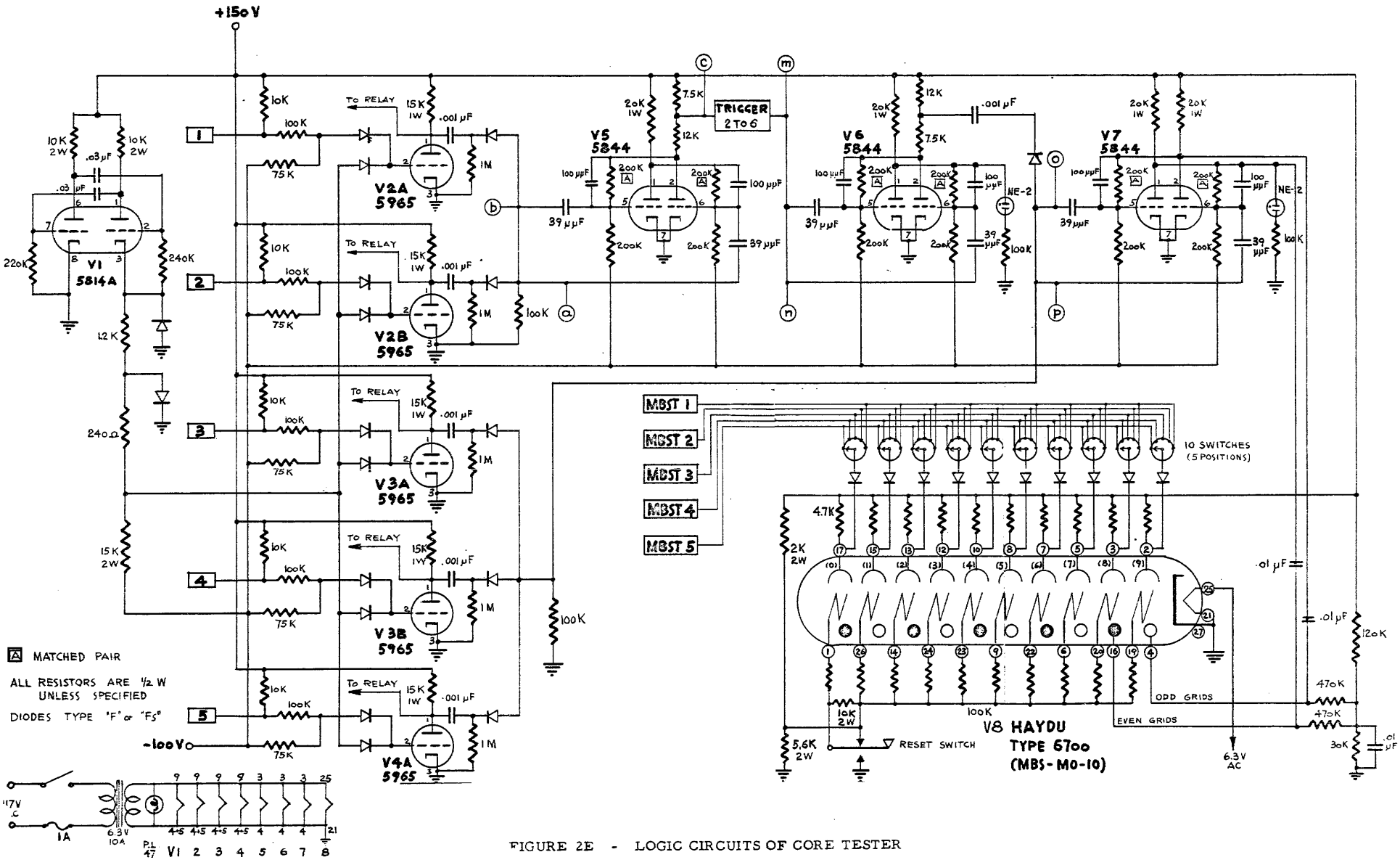


FIGURE 2E - LOGIC CIRCUITS OF CORE TESTER

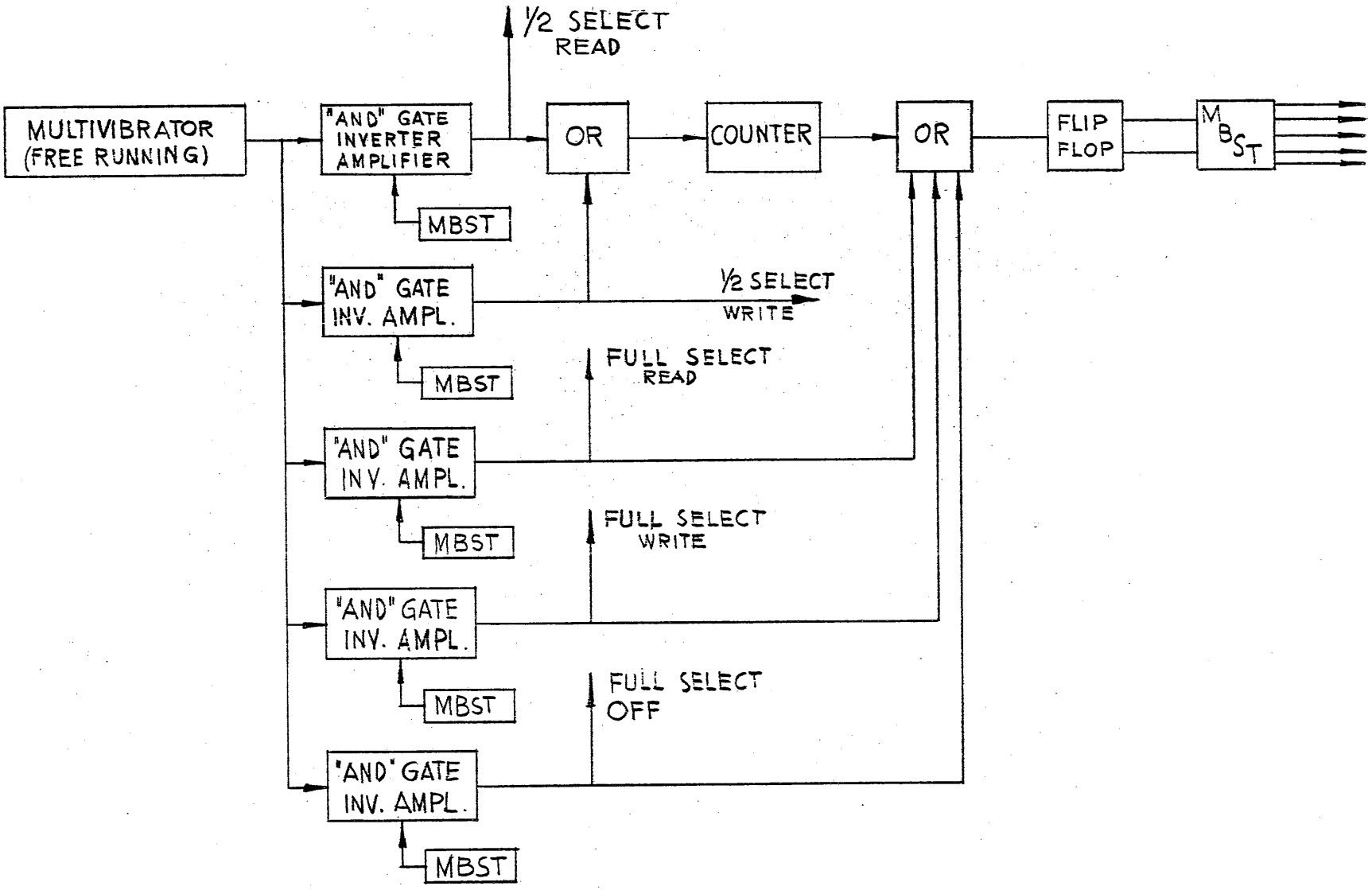


FIGURE 3E - BLOCK DIAGRAM OF CORE TESTER LOGIC CIRCUITS

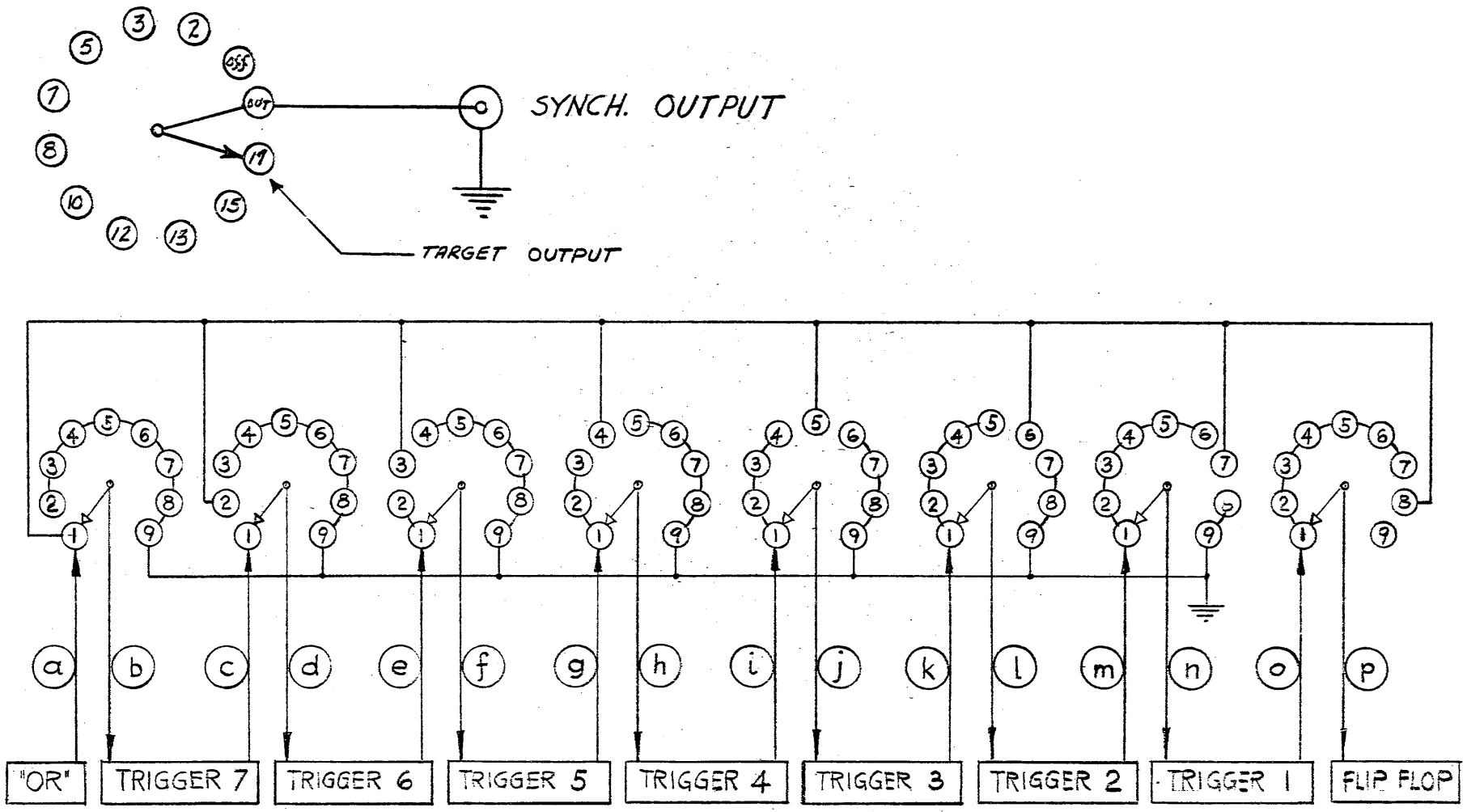


FIGURE 4E - CORE TESTER TRIGGER SELECTION SWITCH

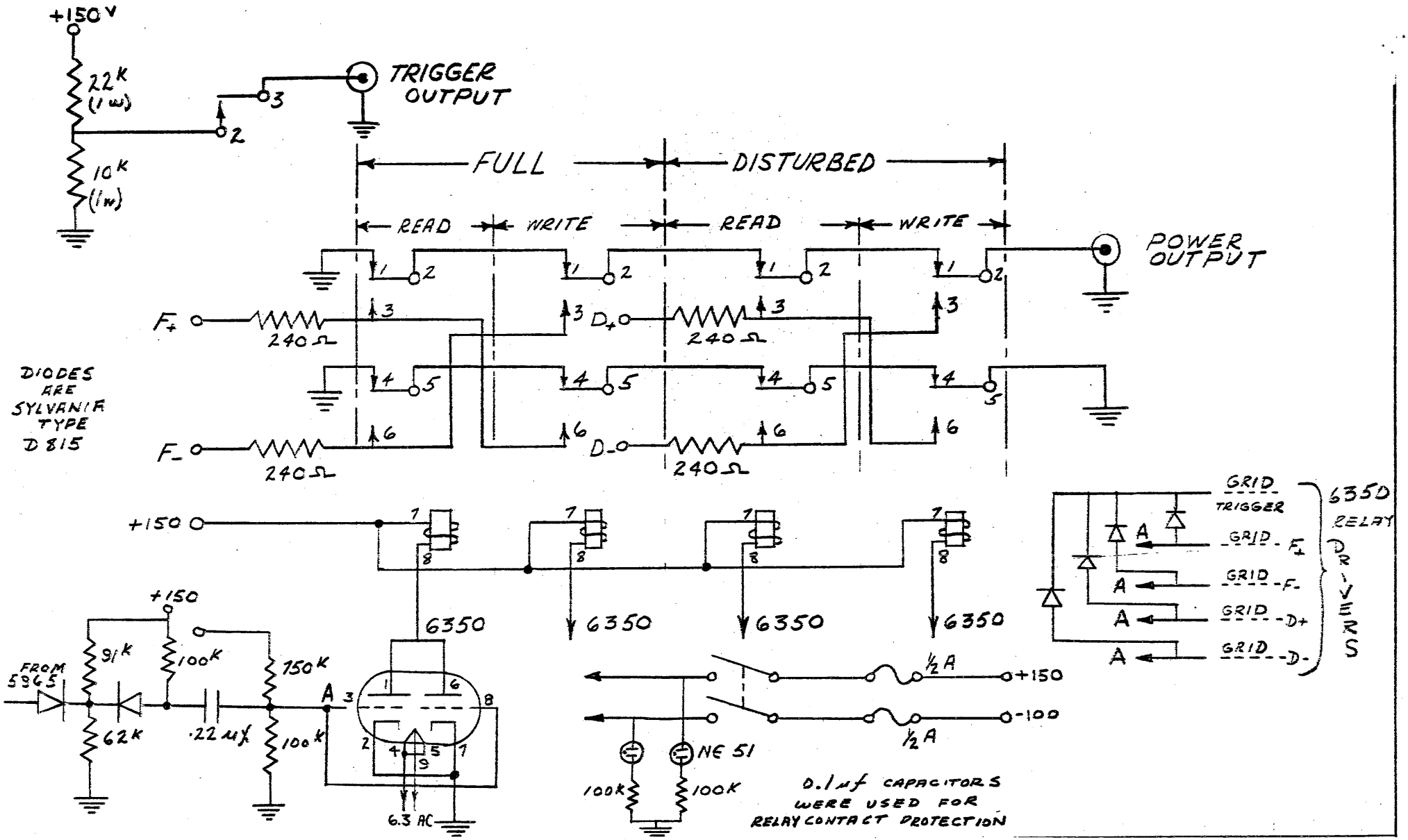
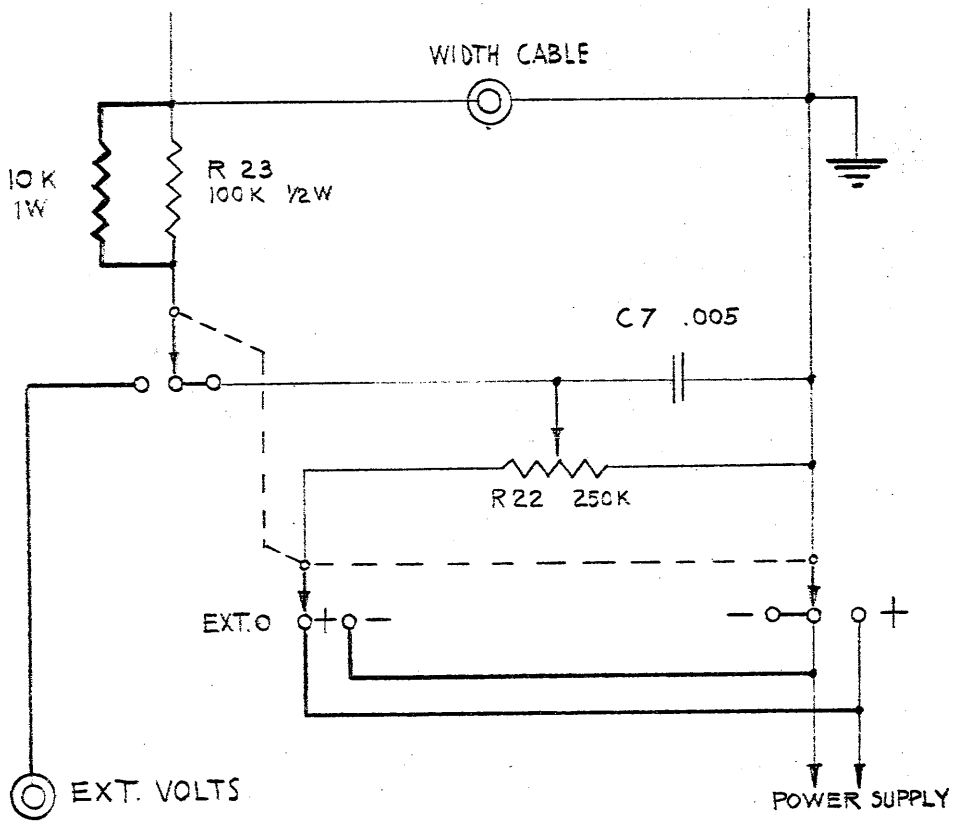
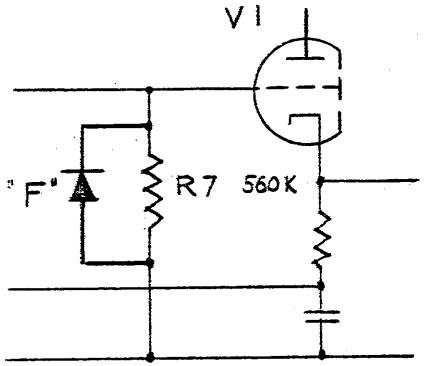


FIGURE 5E - CORE TESTER RELAY CIRCUITS





ADD diode across R7.

Note: Remove old -, +, Polarity switch and install 3-pole, 3 position rotary switch. Drill and mount co-ax connector.

Add 10K, 1 W resistor across 100K.

FIGURE 6E - SKL MODIFICATION FOR EXTERNAL VOLTS

III. F. FAST RISE TIME THYRATRON DRIVER: Designed by P. E. Haddon

The basic circuitry of this driver has been described previously in STM-3, dated 26 June 1956, by P. E. Haddon. The present form of driver unit consists of six thyratron-delay line drivers (see Figure 1F). Two pairs of bipolar drivers accomplish full and half-select read and writing. Another pair of drivers will give inhibit pulses of high and low marginal currents in order that the effects of inhibit pulses on the core operation can be studied.

The schematic in Figure 2F shows the two pairs of read-write drivers. The delay lines are 150 ohm lines built to specific delays as determined by the core testing pulse width specifications.

Figure 3E is a description of the rise time pad which is necessary to slow down the 10 mμs rise time of the drivers.

The inputs to the drivers are from the driver logic unit which provides pulses of sufficient amplitude to fire the thyratrons. Where drive pulses of greater than 2 amps are desired, the supply voltage to the full amplitude drivers must be increased to 700 volts. If any noise is present on the input lines to the grids of the thyratrons, erratic firing will occur. This problem can be eliminated by returning the grids to -130 volts instead of -100 volts.

The triggering time control is used to adjust the position of the write pulse relative to the inhibit pulse when it is desired that both be turned on together. It is possible by means of this control to position a wide inhibit pulse such that it will overlap the write pulse.

The manual handler shown in Figure 1E was constructed in order that it could be immersed in Freon. The small microswitch and relay are required to eliminate arcing of the bias current at the contacts of the core test station.

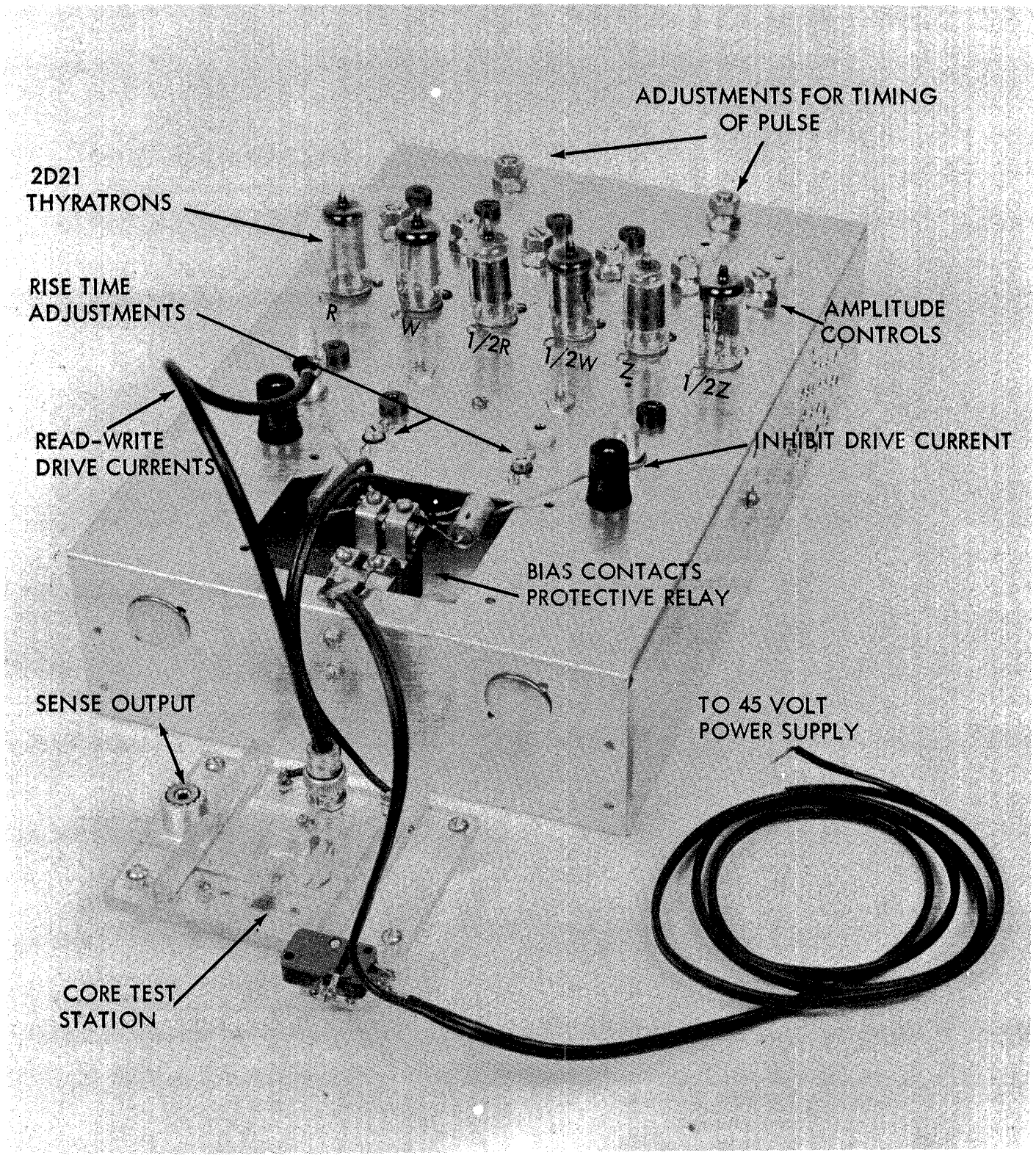


FIGURE 1F - FAST RISE TIME DRIVERS WITH MANUAL 3-HOLE CORE TEST JIG

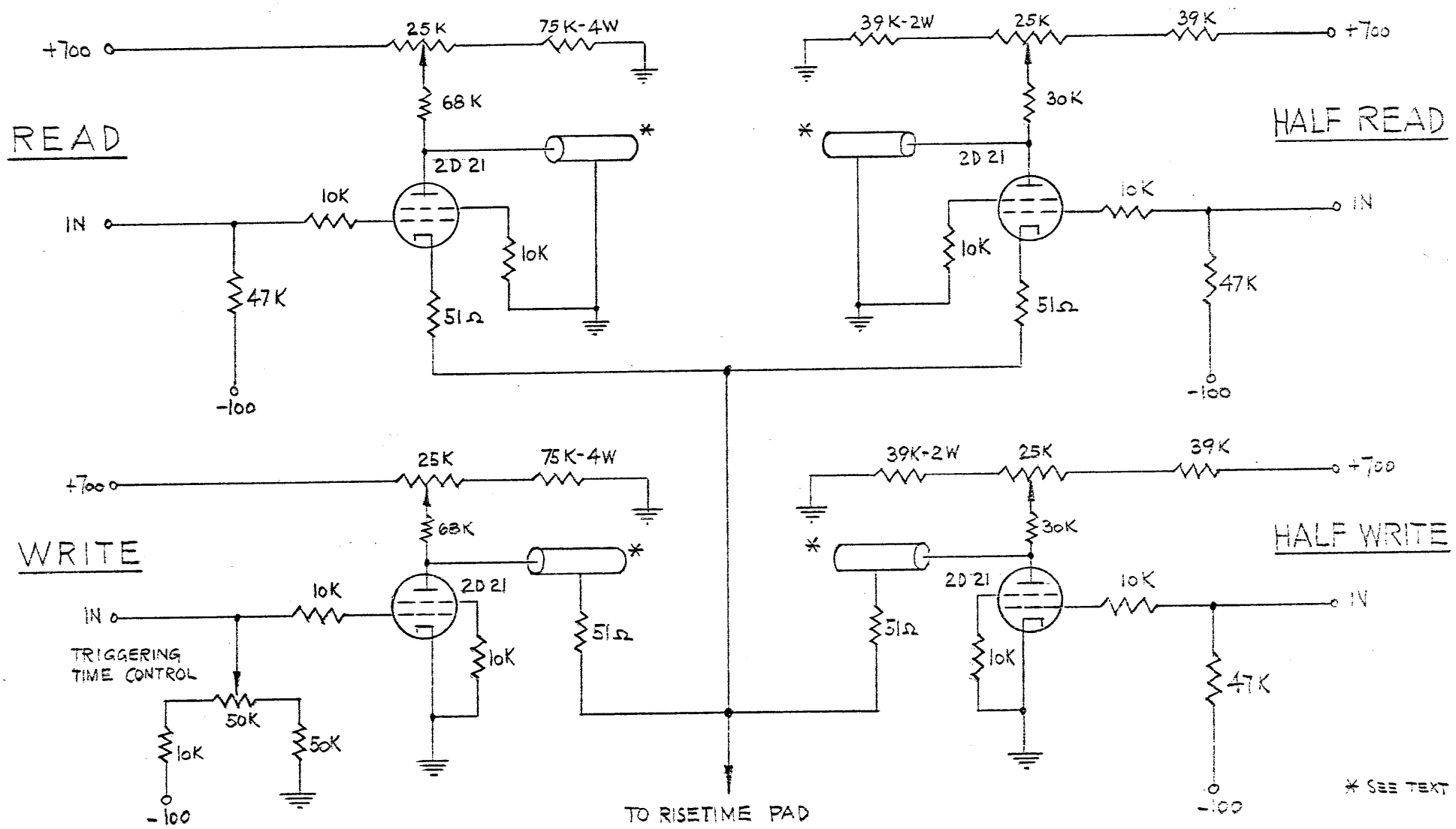
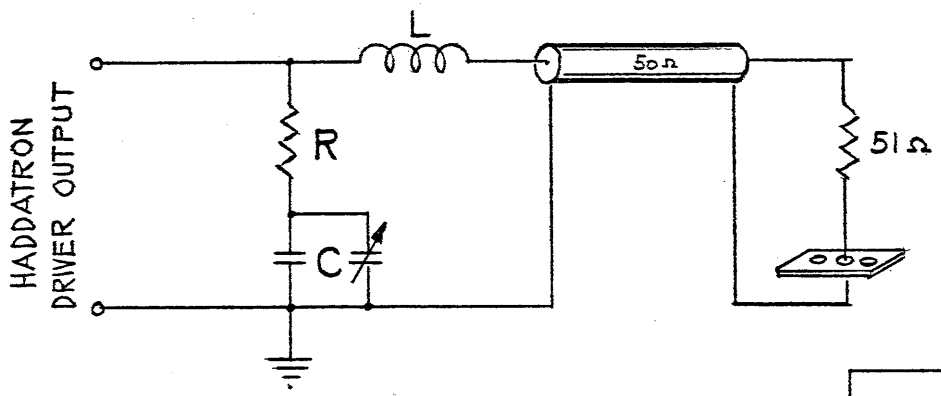


FIGURE 2F - FAST RISE TIME DRIVER



	Rise Time	Calculated Circuit Values		Practical Circuit Values	
	T_R in μsec	L in μh	C in μμf	L in μh	C in μμf
SKL R = 50 Ω	0.050	1.13	452	1.0	470
	0.100	2.26	904	2.0	750
	0.500	11.3	4520	10.0	3900
	1.00	22.6	9040	20.0	7500
THY. R=10Ω	0.050			0.5	330 + 12-125

T_R = RISE TIME 10% TO 90%

$T_R = 2.2 \frac{L}{R}$

$L = \frac{R T_R}{2.2} \qquad \frac{50}{2.2} (T_R) = 22.8 T_R$

$C = \frac{L}{R^2} = \frac{L}{(50)^2} = (4 \times 10^{-4}) L$

FIGURE 3F - THYRATRON AND SKL RISE TIME PAD

III. G. TWO CHANNEL CURRENT DRIVERS: Designed by G.E. Moerschell

This unit is a two channel current driver which has been used for the majority of the work on experimental magnetic core circuitry. It differs from previous hard tube drivers in that it delivers a faster rise, higher current pulse (50 mμs rise and 2.8 amps per channel). A photograph of the unit is shown in Figure 1G.

The driver is programmable from any of the program rings discussed in this report. The pulse duration is variable from 0.5 to 6 μs and can be reduced below 0.5 μs by the use of an "off pulse" which will force a single-shot pulse forming stage to turn off more rapidly.

The maximum allowable average output current for each channel is 800 milliamps. Rise times may be varied from 0.05 to 3 μs. Protective pilot lamps are provided for each channel to prevent overload of driver stages.

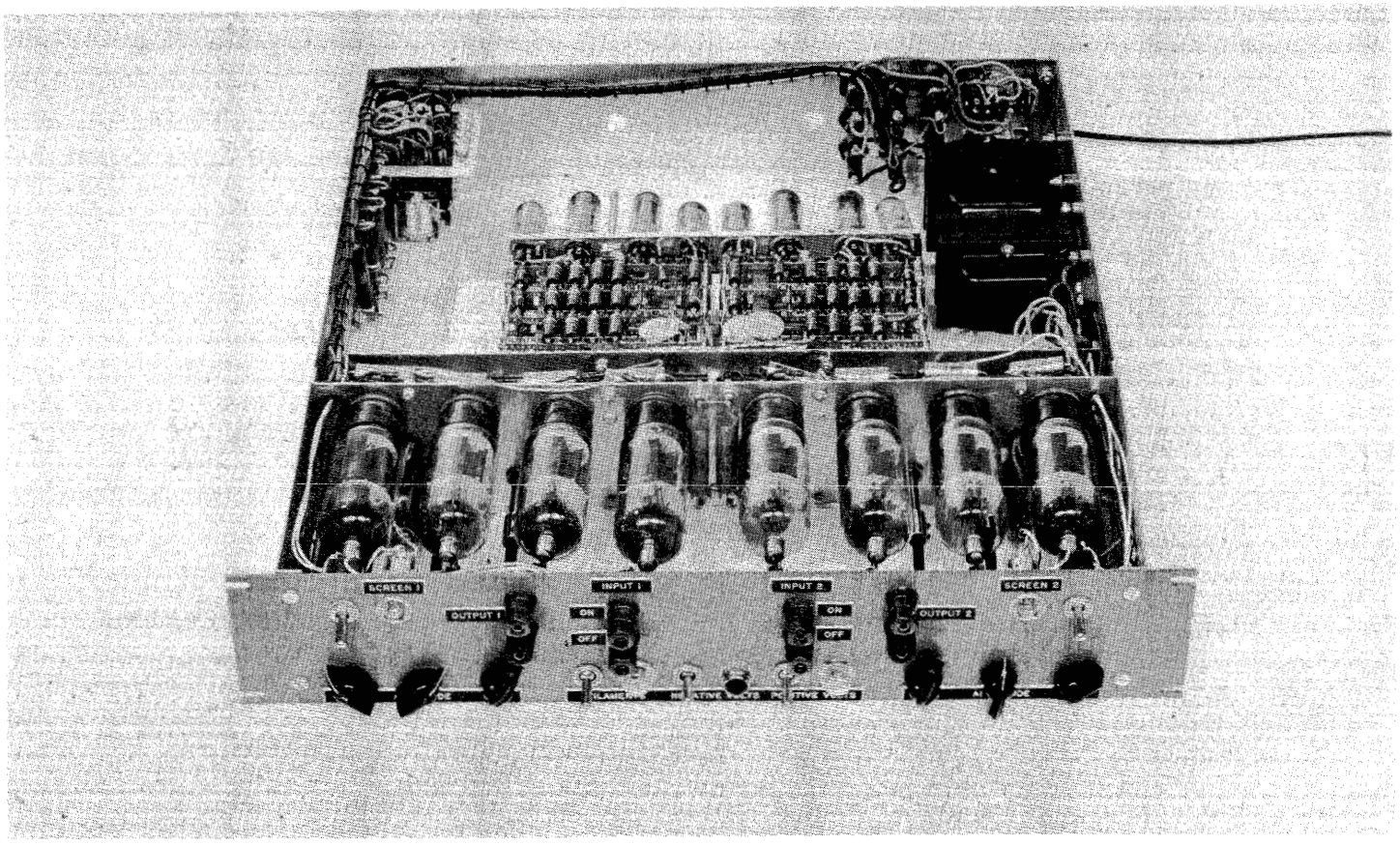


FIGURE 1G - TWO CHANNEL CURRENT DRIVERS