SERIES 7000 CIRCUIT MEMO #13

SUBJECT: A SMALL HIGH-SPEED MEMORY MODEL

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ABSTRACT: The construction and operation of a memory model capable of 0.5-microsecond read-write cycle is described. Included in this report is a summary of data taken pertinent to development of a full-size high-speed memory.

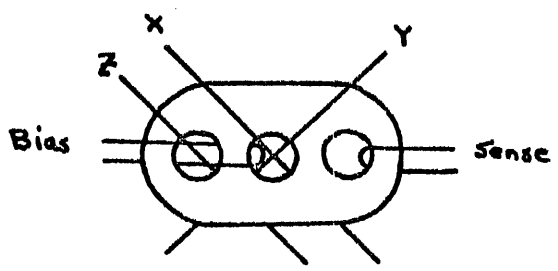
I. Definition and Purpose

The construction of a 256 word, 4 bit, fast memory was undertaken in March, 1957 in order to provide a means of obtaining accurate data on several memory planes operating together. In addition, it was felt that satisfactory operation of this model would show that a full size memory capable of 0.5 microsecond operation was possible. The experience gained by personnel engaged in this project should prove valuable as further work on this type of memory progresses.

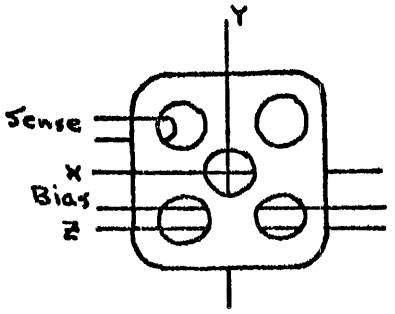
The model consists of 4 planes containing 256 cores each. The cores are arranged in a square matrix with 16 cores per side. The planes were made from a 4 inch square sheet of phenolic which was prepared for core mounting by counterboring holes into which the cores were placed. Spacing between cores is approximately 3/16 inches. The wiring of the array was done manually using No. 36 Formex magnet wire. Spacing between planes may be varied from 1 inch to 1/4 inch.

II. Element and Array Wiring

Three of the four planes contain 5-hole biased multi-path cores and the remaining plane contains 3-hole cores. Each type has inherent advantages and disadvantages which may be briefly mentioned. The primary disadvantage of the 5-hole core is the fact that more drive current is required for the same switching speed as the 3-hole core. The 3-hole core requires that 3 wires pass through at least one hole whereas the maximum number in the 5-hole core is 2. The configuration and wiring of these elements are shown in the sketches below.



3-hole element

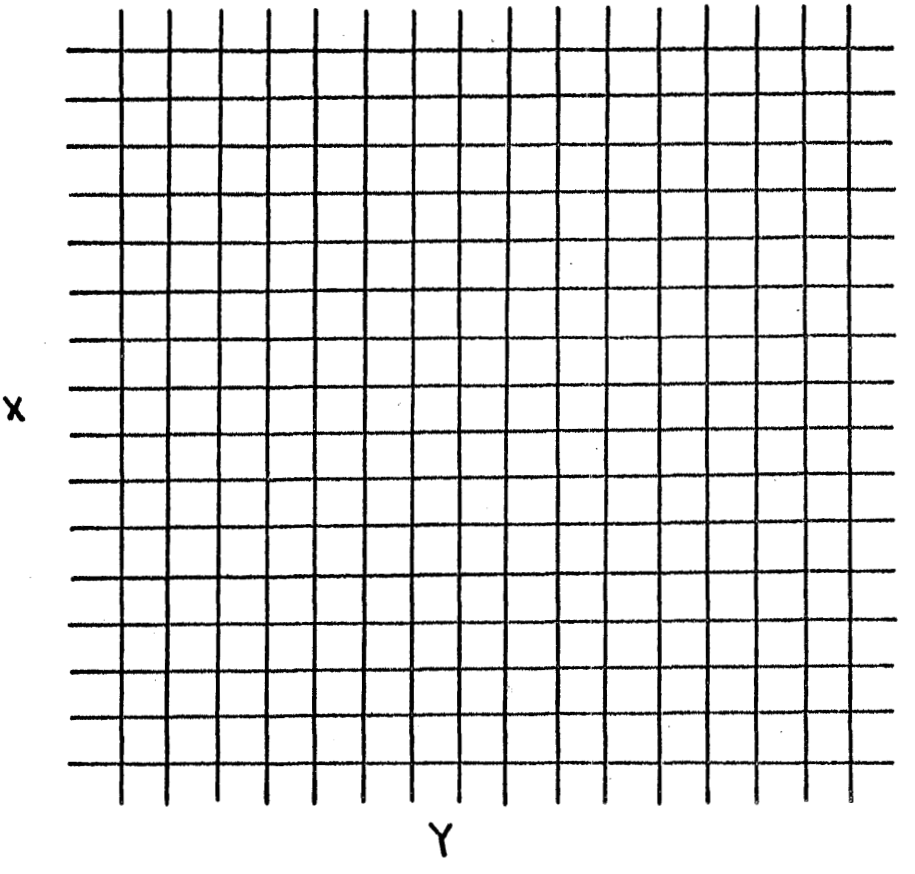


5-hole element

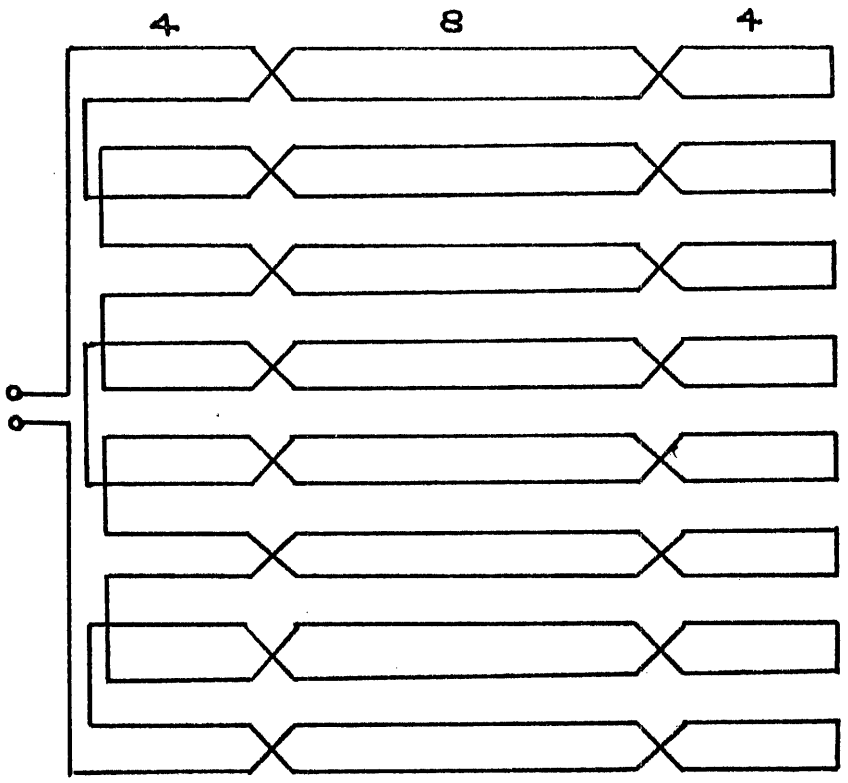
A total of 5 one-turn windings were placed on each core. These are the X and Y drive windings, the Z or inhibit winding, the bias winding, and the sense winding. All are conventional with the exception of the sense winding. The sense winding is of interest because it departs from the widely-accepted diagonal sense winding and becomes a modified type of figure 8 winding. Experiments have shown that this type of winding is superior to the diagonal type in both electrostatic noise reduction and magnetic coupling.

The bias lines of the four planes are connected in series so that only one bias supply was necessary for operation.

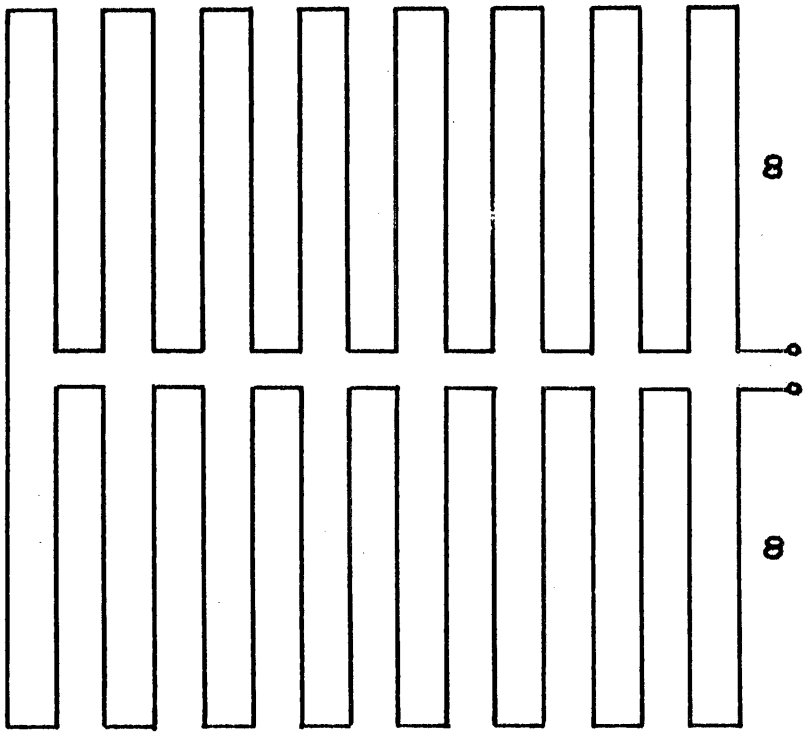
The wiring layouts for the windings used in this array are shown in the following sketches.



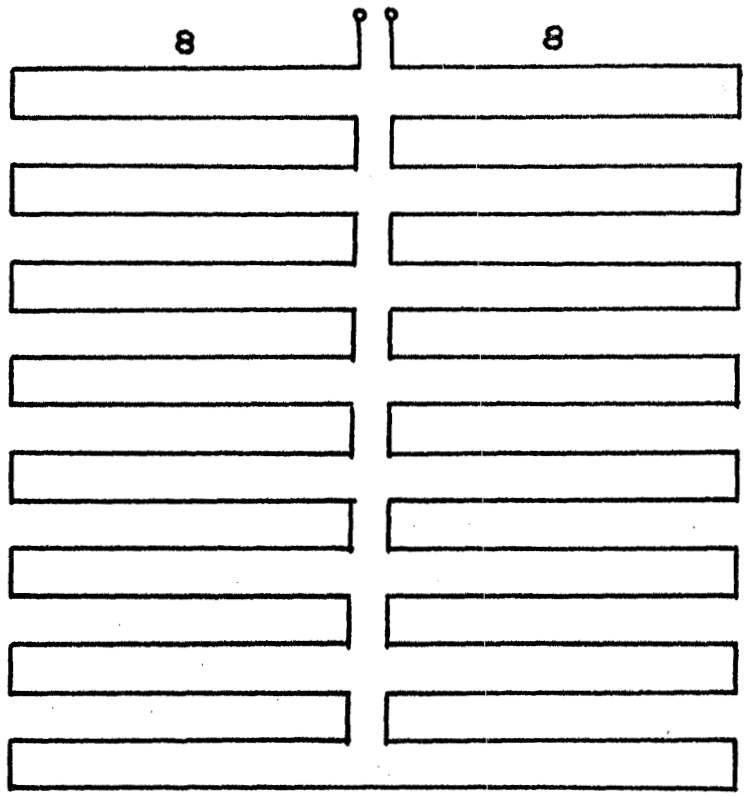
X and Y Drive Lines



Sense Line



Inhibit Line



Bias Line

III. Temperature Stabilization Techniques

It has been long established that ferrite materials are sensitive to temperature. As the temperature of a ferrite core is increased toward the Curie Point, the flux density decreases until, at the Curie Point, the ferrite becomes paramagnetic. With constant drive applied to a core, the switching time decreases with temperature rise. The changing of these parameters results in a wide variation of core output voltage.

The rapid switching time and high pulse repetition rate encountered in a 0.5-microsecond memory cycle cause a relatively high power dissipation per unit volume. If the core were operated in air, a few seconds of sustained switching at one address would cause a core temperature rise which would result in degeneration of core output. Rapid heat transfer was effected by evaporative cooling, a technique widely used in electronic applications which require a fairly constant ambient temperature.

The entire array was immersed in a tank containing trichloromonofluoromethane (CCl_3F), a chemical also known under the DuPont trande name of Freon 11. The range of core temperature operation was restricted between the limits of the bath temperature (approximately 20°C) and the boiling point (23.8°C at 1 atmosphere).

Cooling coils were provided which removed the heat from the CCl_3F vapor, allowing condensation and reuse of the chemical.

IV. Driving and Sensing

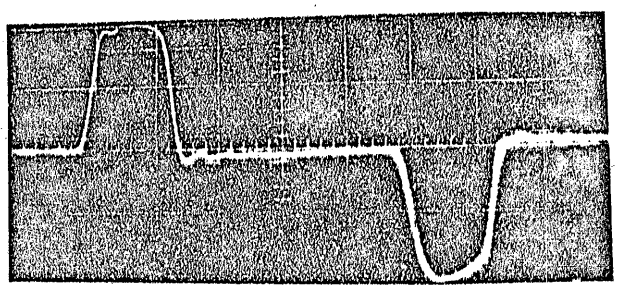
A 16-output G-0.5 switch was available for selecting a given X-line. This switch was designed for use with transistor current drivers; however, the lack of a sufficient number of suitable power transistors necessitated the use of vacuum tube drivers. The Y-line was driven by a ferrite switch core. Another switch core was also available for driving the X-line when the G-0.5 switch was not used.

Word selection with switch core drive was done with external jumpers on the outside of the tank.

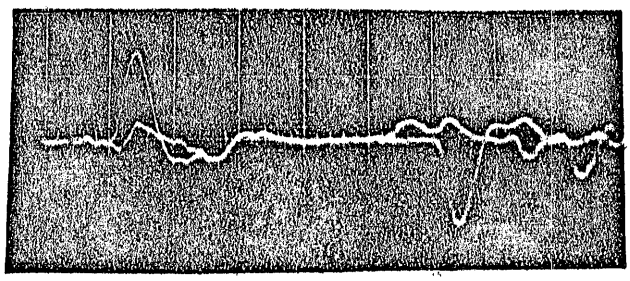
Inhibit pulses were supplied with vacuum-tube constant-current drivers. The D.C. bias source was a vacuum-tube constant-current supply. Timing pulses were obtained from a delay-line ring driven by a commercial pulse generator.

A sense amplifier has not yet been used with this model. Observation of the sense line outputs was made with a 545 Tektronix Oscilloscope with a Type 54/G Wide-Band Differential Amplifier. The differential amplifier was used to eliminate common mode noise for ease of viewing.

Photographs of current pulses into the array and the core outputs resulting from them are shown below. The pulse repetition rate was approximately 500 KC at the time these pictures were taken. The plane being sensed contained 5-hole elements.



Input Current Pulses
0.5 amp/cm 0.2 μsec/cm 50 mμsec rise time



Core output voltage as seen on sense line
Read 1, Write 1 superimposed on Read 0, Write 0
0.2 volts/cm, 0.2 μsec/cm

V. Array Measurements

The table shown below lists measured values of characteristic impedance and time delay of the various lines. All measurements were made with the cores in a biased condition with uni-polar pulses applied.

	Z_o ohm	T_d mμs	No. Cores
X or Y	170	12	64
Z	130	22	256
Bias	220	90	1024
Sense	180	21	256

Tolerances on the measurements of characteristic impedance are in the range of $\pm$ 10 ohms.

All lines with the exception of the X and Y show a delay of about 100 mμsec per 1000 cores. The X and Y line delay appears to be appreciably higher. It is felt that the small number of cores per line and the relatively longer length of connecting wires to the top of the tank introduced enough error to appreciably affect the accuracy of the measurements. There is no apparent reason why the delay in the X or Y lines should be appreciably different from the other lines.

Back voltage on the bias line was approximately 23 volts peak to peak. This measurement was made with cores switching at one address to yield maximum back voltage.

Common mode noise was found to be 3.5 volts peak to peak on the sense line without the inhibit driver on. With the inhibit driver on, this voltage increased to 9 volts peak to peak. This common mode noise was many times larger than a typical core signal from a good address, the latter being about 0.3 volts for a one and 0.07 volts for a zero in a 5-hole core plane.

VI. Conclusions

This model has been operated satisfactorily at repetition rates of slightly above 1.5 MC. Erratic current driver operation at high PRF has thus far prevented successful operation of a 0.5 microsecond cycle.

The data acquired thus far has been useful in evaluation of the planned memory and should in further development.