STRETCH CIRCUIT MEMO #3

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SUBJECT: Millimicrosecond Non-Saturating Transistor Switching Circuits.

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SUMMARY: New techniques for switching well specified currents with small associated voltage swings, using non-saturating techniques, have been developed.

Cumulative delays through sequential logical stages, using commercially-available high-speed transistors, average 12 millimicroseconds.

INTRODUCTION

There are four primary limitations on the speed of transistor non-saturating circuits. These are:

1. The limitations imposed by transistor and other circuit capacitances. Assuming a current step into a node, the voltage rise time is directly proportional to the product of the required voltage swing and the capacitance to ground at the node.

2. α cut off frequency.

3. Storage time in associated diodes.

4. Diffusion delay.

When transistors, having cut off frequencies of several hundred megacycles are considered, circuit capacitances become the primary limitation on the speed of transistor circuits.

A mode of operation is being investigated in which well specified currents are switched with small associated voltage swings, thereby reducing the limitations imposed by circuit capacitances. This method is considered potentially fast and reliable.

BASIC SCHEME OF OPERATION

The voltages, currents, and resistors for the circuits described in
this report were chosen for use with Philco Surface Barrier Transistors.
The configurations presented may be adapted and optimized for use
with many types of transistors.
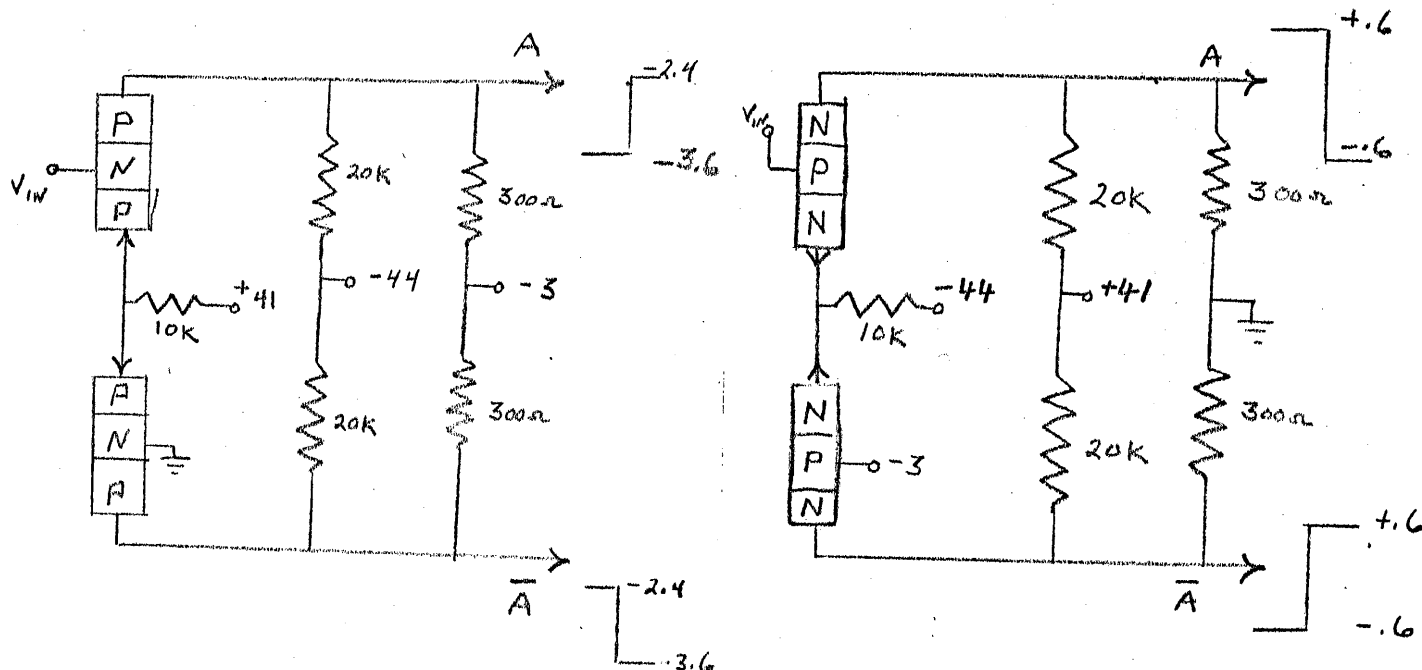
For the PNP circuit, shown above, assume that the input signal is at
$+0.6$ volts. The bottom transistor will be conducting and for a max-
imum drop across the conducting emitter of $+0.4$ volts, the emitter
of the top transistor will be reverse biased by 0.2 volts. Assuming
a maximum drop across the conducting emitter of 0.4 volts and a
minimum drop of 0.2 volts, and for α ranging from 20 to ∞, the
collector current of the bottom transistor will vary between the
limits of 3.86 to 4.08 Ma $+ I_{co}$. The collector current of the top
transistor will be I_{co}.

When the input signal is at -0.6 volts the top transistor will be con-
ducting and for a maximum drop across the conducting emitter of 0.4
volts, the emitter of the bottom transistor will be reverse biased by
0.2 volts. For the same tolerances, as given above, the collector
current for the top transistor will vary between the limits of 3.92 to
4.12 Ma $+ I_{co}$. The collector current of the bottom transistor will be
I_{co}.

The variations in output currents mentioned above do not include variations due to resistor and power supply tolerances.

For the PNP circuit there are two outputs which are complements of each other and are ideal for driving the NPN equivalent.

The time constants determining the transient behavior of the output currents for both the top and the bottom transistors, for an applied voltage step at the input, approach the time constants for a grounded base amplifier. Since the collector load resistances are small, the speed of response to an applied voltage step approaches the theoretical limit of the transistor.

A METHOD OF DOING LOGIC

The basic scheme of operation points out that PNP collectors must drive NPN bases, and NPN collectors must drive PNP bases. It is contemplated that there will be logical blocks having all PNP inputs, or all NPN inputs, or combinations of both types.

In any system there will be both N lines (NPN driving PNP) and P lines (PNP driving NPN). A logical one exists on a P line when its potential is at its most positive level. A logical one exists on an N line when its potential is at its most negative level.

The advantage of this notation is as follows. If, in any logical block, the following exchanges are made; PNP transistors and NPN transistors, -44 volts and +41 volts, -3 volts and ground, the resulting logical block retains the original logical statement.

If another notation should be used (such as all up levels are logical ones), a particular configuration would have a different logical statement depending on whether its inputs are on P lines or N lines. Although no additional configurations would be necessary to perform all logical functions, the choice and application of a particular configuration would depend on the input lines available.

SOME TYPICAL CIRCUITS

In any of the circuits shown, PNP and NPN transistors may be inter-changed providing the voltages are interchanged as described above. Each circuit shown has a counterpart using transistors of the opposite kind and having the same logical function.
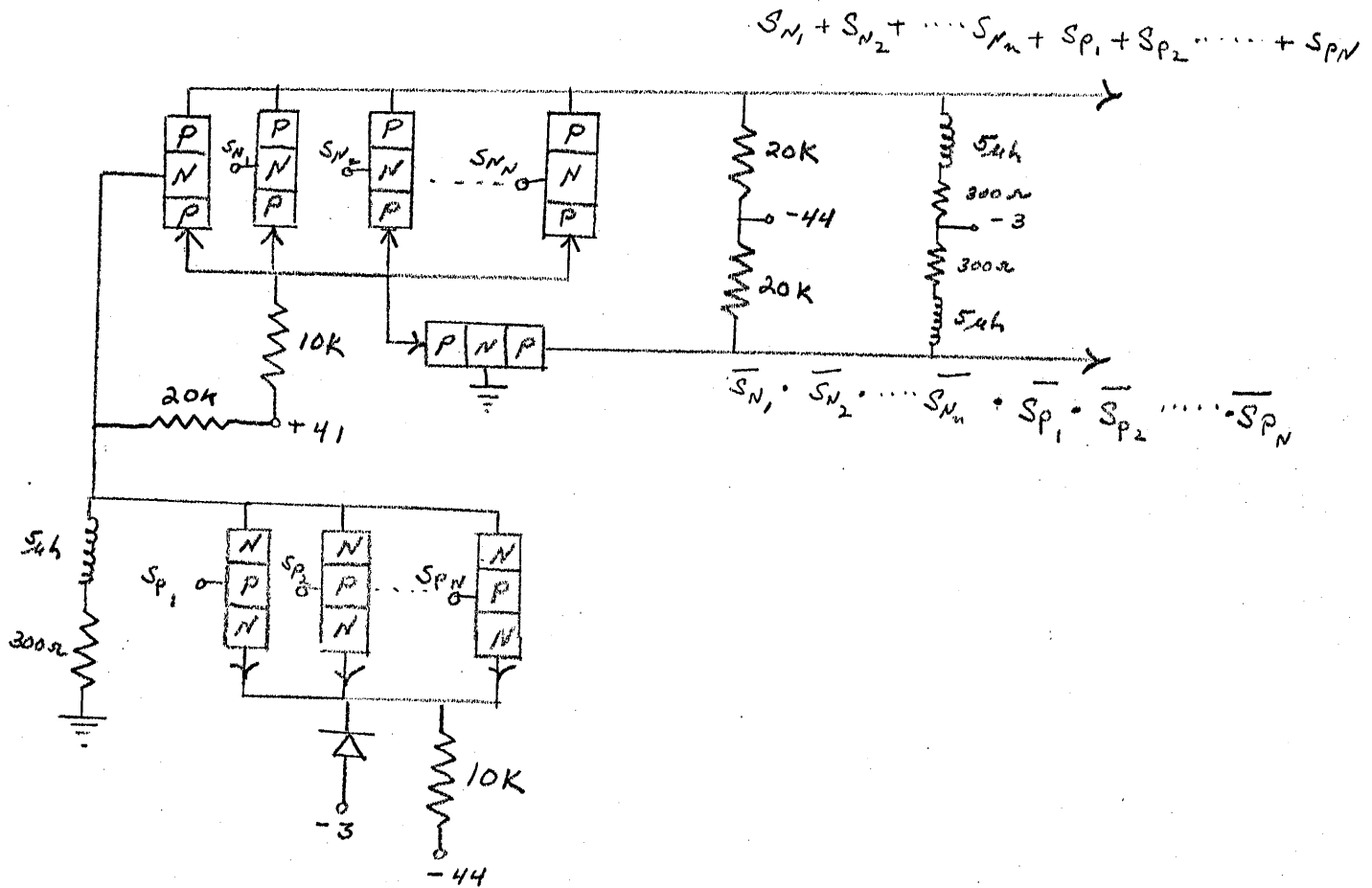
The n way complemented "Or" circuit using inputs from transistors of one type.

Since complements are always available, the n way complemented "Or" circuit can perform all "And" or "Or" operations on n signals or their complements.
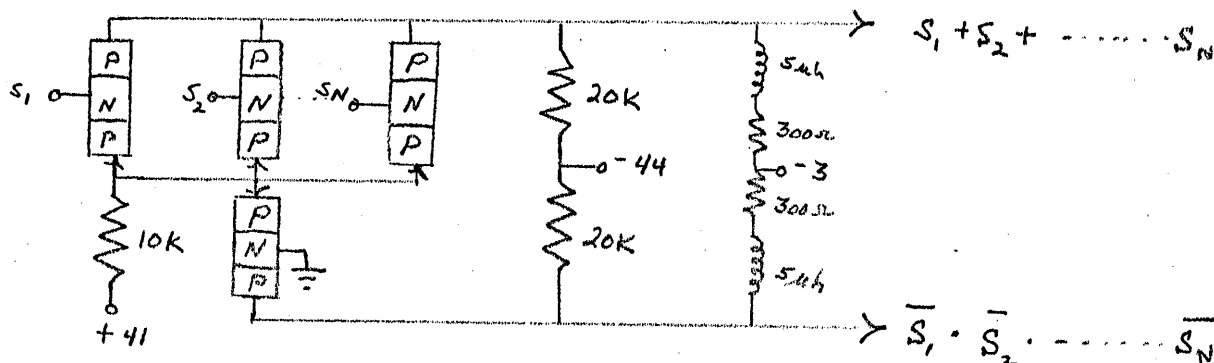
If the complement for the above circuit is not required, the bottom transistor may be replaced by a diode.
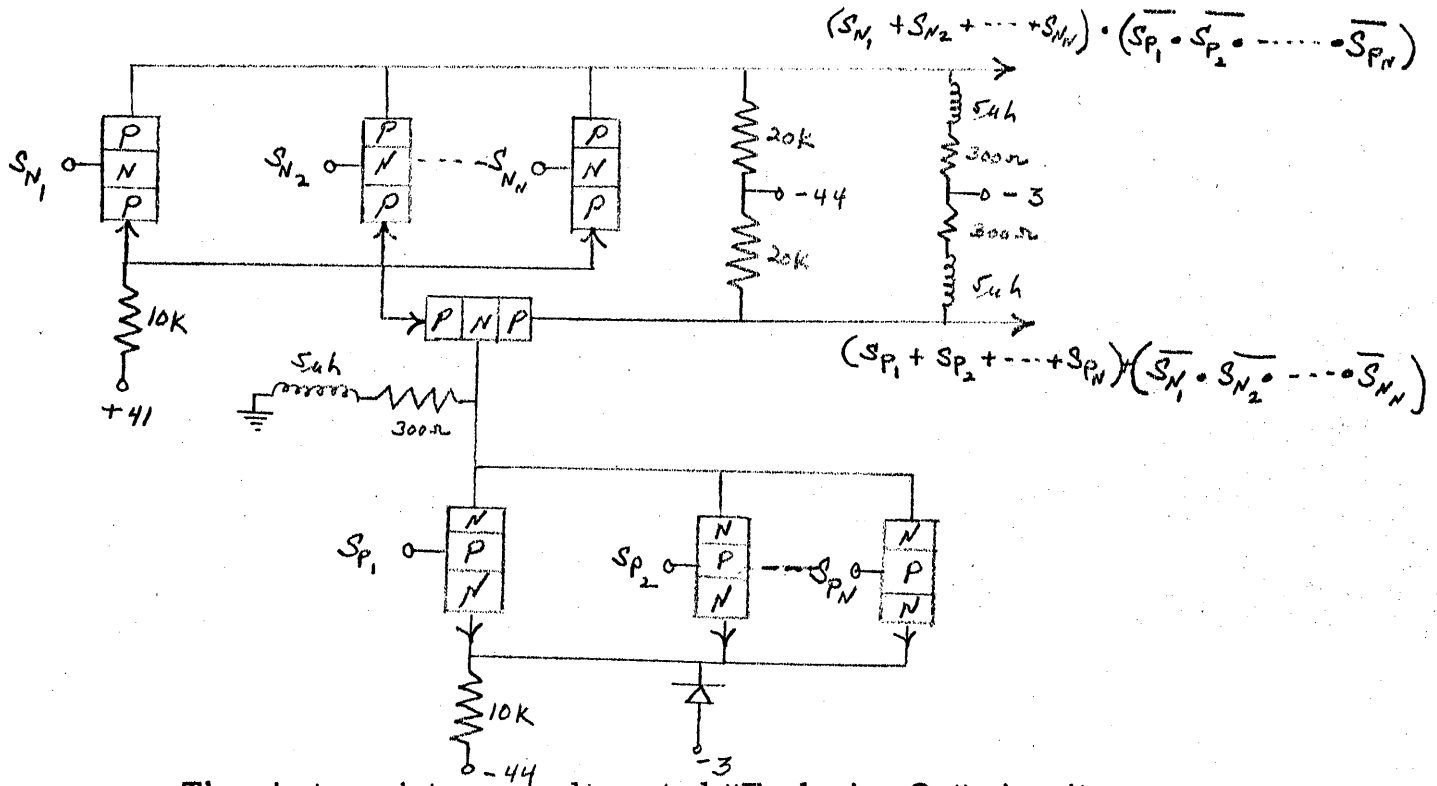
The n way complemented "Or" circuit using inputs from transistors of both types.

$$S_{N_1} + S_{N_2} + \cdots S_{N_n} + S_{P_1} + S_{P_2} \cdots \cdots + S_{PN}$$

$$\overline{S_{N_1}} \cdot \overline{S_{N_2}} \cdots \overline{S_{N_n}} \cdot \overline{S_{P_1}} \cdot \overline{S_{P_2}} \cdots \cdots \overline{S_{PN}}$$

The circuit shown above consists of a combination of an all
PNP complemented "Or" circuit, and an all NPN uncomplemented
"Or" circuit. The circuit requires one more transistor than
a complemented "Or" circuit using one type of transistor, and
introduces the additional time delay of one logical block.
Careful layout of a system should minimize the need for this
type of circuit.

The complemented (A $\neq$ B $\neq$ C $\neq$ -----) . ($\overline{E}$. $\overline{F}$. $\overline{G}$. -----)
circuit having inputs to both types of transistors.

This circuit makes use of inputs to the bases of both the top
and bottom transistors of the n way complemented "Or" circuit.
The requirement for an impedance at the base of the bottom
transistor may result in a slight sacrifice in speed.

$$(S_{N_1} + S_{N_2} + \cdots + S_{N_N}) \cdot (\overline{S_{P_1}} \cdot \overline{S_{P_2}} \cdots \cdot \overline{S_{P_N}})$$

$$(S_{P_1} + S_{P_2} + \cdots + S_{P_N}) (\overline{S_{N_1}} \cdot \overline{S_{N_2}} \cdots \cdot \overline{S_{N_N}})$$

The six transistor complemented "Exclusive Or" circuit.

$$A \cdot B + \overline{A} \cdot \overline{B}$$

$$(\overline{A} \cdot B) + (A \cdot \overline{B})$$
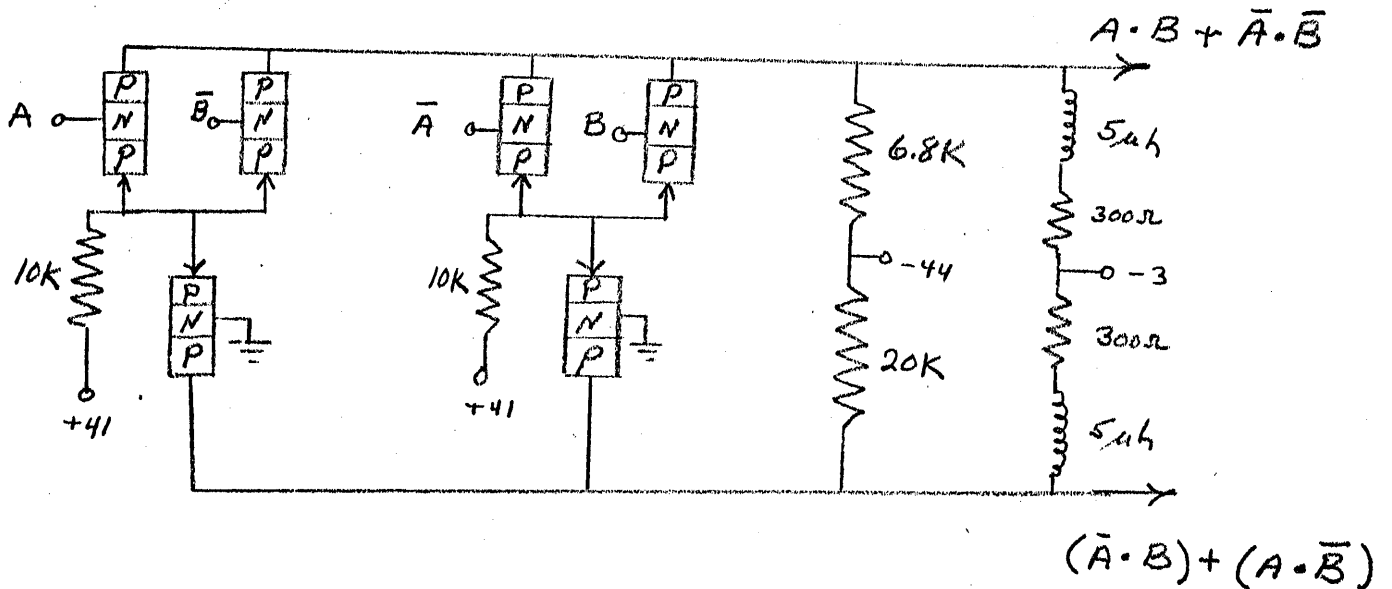
The four transistor complemented "Exclusive Or" circuit.
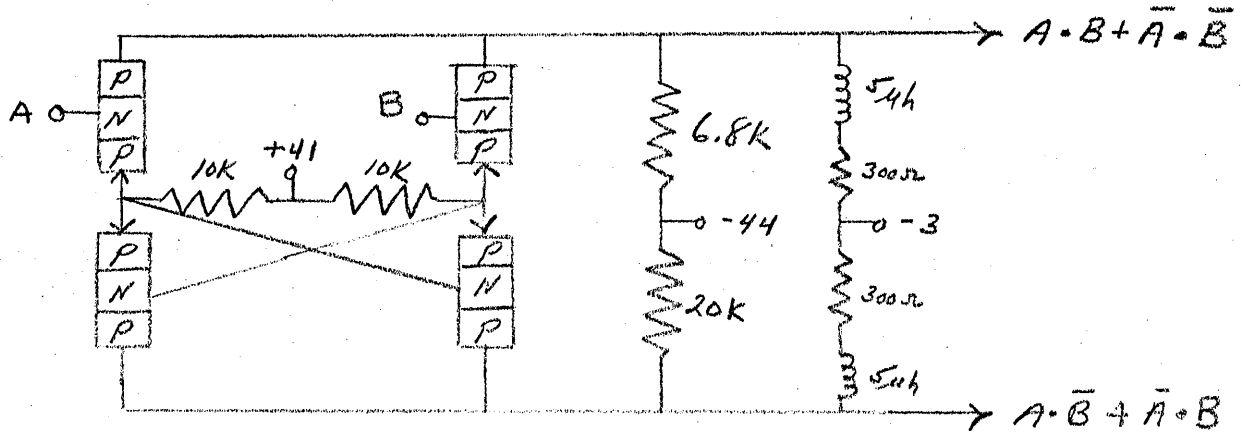
This circuit requires tighter tolerances on transistor emitter characteristics, but may be useful where transistors having uniform emitter characteristics are available.

TRIGGERS

Several triggers are presently under investigation. Three bistable devices, without gating circuits, are presented below.
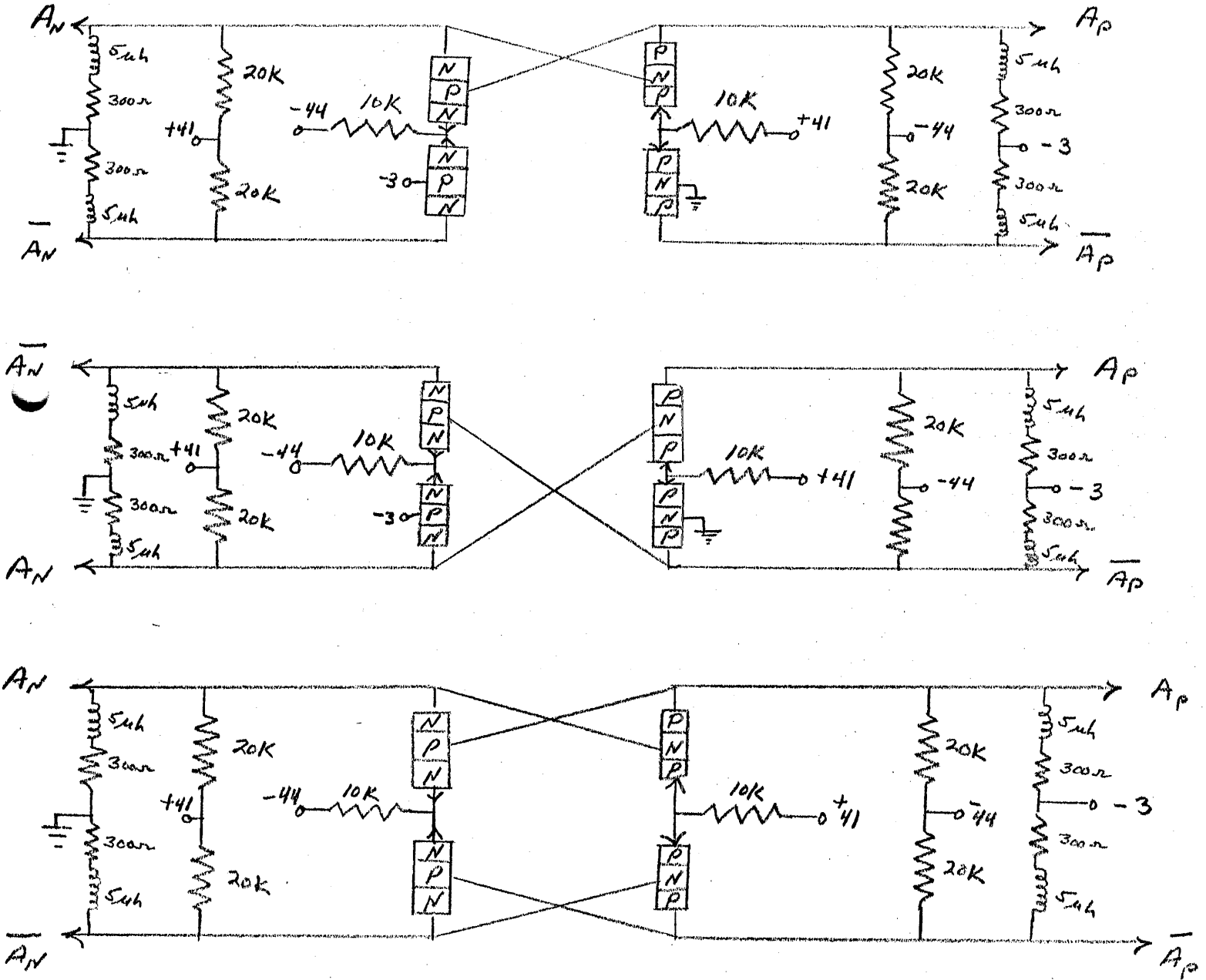
DRAWBACKS AND POSSIBLE SOURCES OF TROUBLE

All the possible difficulties involved in the proposed scheme cannot come to light unless an effort is made to construct a fairly large system. Some of the possible difficulties that are apparent at this time are described below.

1. The need for both NPN and PNP transistors.

2. Emitter breakdown voltage.

   The circuits described require a minimum emitter breakdown voltage of 1 volt. This may be difficult to obtain with high speed graded base transistors.

3. Noise.

   Pick-Up: Since impedance levels, at a ll nodes, are less then 300 ohms, noise due to pick-up should not be severe.

   Noise on the power supplies: Noise on the ╋41 and -44 volt supplies should cause little trouble. Noise on the -3 volt supply and ground, which is common throughout the system, should cause little trouble.

   Noise on the -3 volt supply of an NPN logical block, which is not common to the noise on the -3 volt supply of the PNP block which is driving it, could cause trouble.

   Noise on the ground line of a PNP logical block, which is not common to the noise on the ground line of the NPN block which is driving it, could cause trouble.

This indicates that it would be desirable that logical blocks and the blocks driving them be mounted close together.

Where it is necessary that the output of a logical block drive another
block located at a considerable distance, the following scheme may
be useful.
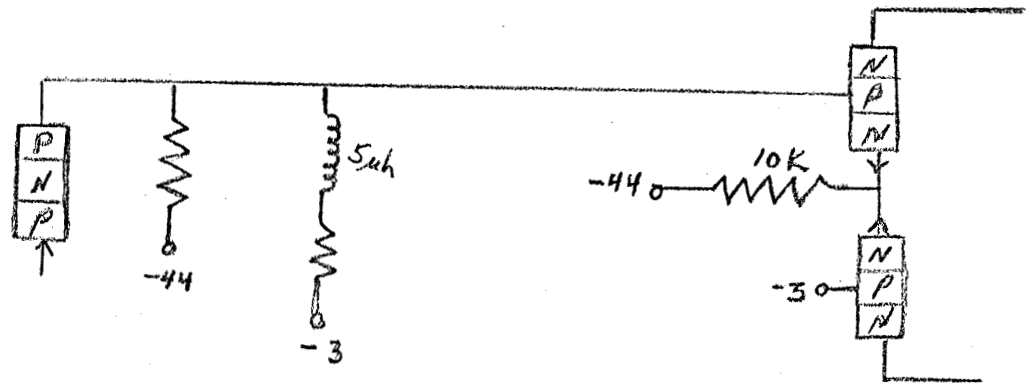
The sketch shown above is that of a PNP collector driving a NPN base
at a distance. Noise on the separated -3 volt supplies could cause
trouble. Contact resistance and resistance of the line could cause some
level shifting to occur. If the combination of resistors and the inductance
are moved to the NPN block as shown below,
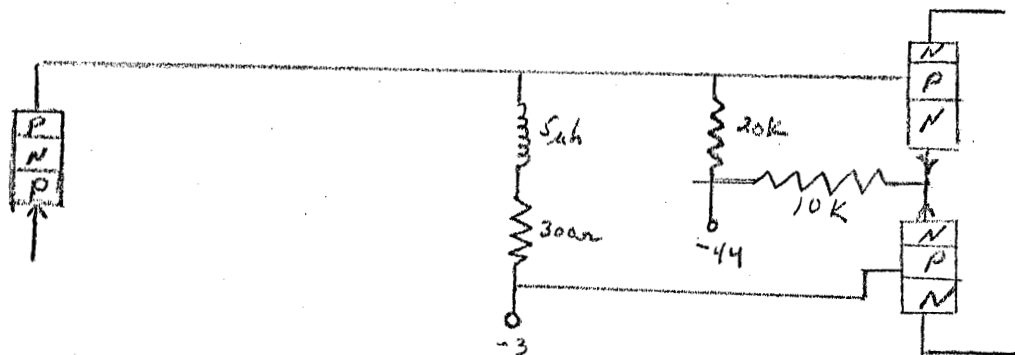
the -3 volt supplies are now the same. Since current rather then voltage
is now being transmitted, there can be no d-c level shifting. A further
advantage is that the impedance at the end of the line is now in the vicinity
of the characteristic impedance of a high frequency transmission line.

A WORKING EXAMPLE

A small system was constructed in which two-way complemented "Or" circuits were cascaded. The output of each complemented "Or" circuit was driving two other "Or" circuits. Because of a shortage of high speed NPN transistors the "Or" circuits were constructed using Philco Surface Barrier Transistors and the circuits were coupled through grounded base NPN buffer stages. General Electric ZJ7-1 NPN tetrodes were used for the NPN buffer stages.

For the photograph shown below, the time base is 50 millimicroseconds/cm and the voltage calibration is approximately 1 volt/cm. The photograph was taken on a Tektronix 517 Oscilloscope. The upper waveforms are the input waveforms to the first of four cascaded "Or" circuits. The lower waveforms are the output waveforms of the last circuit. The delays observed include the delays of the grounded base buffer amplifiers.

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