

Griffell

COMPANY CONFIDENTIAL

August 21, 1957

Exchange Memo #22

Input Output Memo #3

SUBJECT: Byte Converter

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General Description

A byte of information to or from Exchange consists of 8 bits of data and a check bit. A character on tape consists of 6 bits of data and a check bit. The byte Converter presents a means of converting from one format to the other.

The Byte Converter can be constructed as an integral part of the Control Unit and will require 505 transistors, or approximately 36 large cards and 85 small cards.

The Byte Converter can also be constructed as an independent auxiliary unit, operating into a basic Control Unit and will require no additional control lines to the Exchange. It will require 8 additional lines to the Control Unit and 211 additional transistors.

Operation of the unit is based upon a core plane capable of storing 24 bits of data, with facilities for reading in and out at the proper timings and in the proper groupings. Both inputs are checked for vertical redundancy, The outputs are checked by an odd-even comparison of the input and output check bits.

Detailed Description

When writing, the Exchange sends 8 bit bytes to the Tape Control Unit and the Control Unit must cause 6 bit bytes to be written on tape. When reading, the Tape Unit sends 6 bit bytes to the Tape Control Unit and the Control Unit must cause 8 bit bytes to be delivered to the Exchange. Thus, there is a need for 8 to 6 and 6 to 8 conversion in the Tape Control Unit.

Since the Read and the Write Converter are similar in operation only the Read operation, will be described. The attached diagram illustrates this description.

When Reading the output of the six bit register is fed into the Core matrix write drivers which causes a half write driver current in each of the vertical write lines corresponding to a "1" bit in the read register. Coincidentally a half write current is fed through a select diagonal so that the bits of information are stored along the diagonal which has been selected. The first six bit byte is written into the diagonal identified as 1 RI. The second, third and fourth bytes are written into the diagonals 2RI, 3 RI, and 4RI respectively. The first eight bit byte of information is read out of the cores by applying full current on the diagonal identified as 1 RO. The second and third bytes are formed by applying full current to the diagonals 2 RO and 3 RO respectively.

During both Reading and Writing operations the timing for the read-in and read-out has been arranged to equalize the frequency of occurrence.

On both read and write, a parity bit check is utilized to carry the checking procedure around the converter and provide a check on operation of the converter itself. Both the input and output check bits are added to an odd-even trigger and at the end of a record the trigger is sampled to be sure the results are even. An odd count indicates an error.

If the Byte Converter is built as a part of the Control Unit, the 6 write register can be the original Control Unit write register and the 8 read register can be the original Control Unit read register with one position added.

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The two redundancy checkers can be the ones in the original Control Unit. However, if the Byte Converter is built as a separate unit these items must be duplicated in the Byte Converter.



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