COMPANY CONFIDENTIAL

June 20, 1957

Exchange Memo No. 19

SUBJECT: Organizational Consideration in the Stretch System to allow operation of High Speed Exchange.

REFERENCE: Stretch File Memo No. 61

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The reference memo includes cases showing access time to the 2.0 usec memories from the Exchange for both reading and writing. These times are based upon the Basic Exchange having priority in access to the memory. When reading a word from memory the Basic Exchange will get the word in 4.5 usec in the worst case and can write a word to memory in 1.2 usec in the worst case with the bus system as proposed.

The average word rate of the High Performance tape at 100 times 727 bit rate is calculated to be 7.1 usec per word and for High Speed Disks to be 8 usec per word. Proposed organization of the system calls for one high performance unit to be reading and one writing simultaneously.

Let us assume for the moment that the Basic Exchange will never conflict with the High Speed Exchange in requesting memory usage and further that the High Speed Exchange also has priority in access to a memory. When simultaneously reading and writing and assuming the worst case which is then the same as described above, word transfers for the High Speed Exchange will occupy 1.2 + 4.5 usec or 5.7 usec out of every 7.1 or 8 usec cycle depending upon whether we are operating with tape or disk. Assuming a 10% speed variation on tape the time would fall within that required for reading and writing simultaneously.

Let us next assume that the Basic Exchange can conflict with the High Speed Exchange in obtaining access to a memory, i.e., there is

no attempt made to allocate particular blocks of memory to the two Exchanges. In this case a minimum of 2.3 usecs must be added to both the reading and writing times. The organization of the bus system to provide first and second priority for the Basic and High Speed Exchange has not been postulated. Therefore, the 2.3 usecs takes into account only the additive effect of the Basic Exchange taking main memory cycles in step with the High Speed Exchange and computer and does not include any bus times. This worst case can continue for an indeterminate number of cycles. This would result in an increased word transfer time for the High Speed Exchange of 10.3 usec per cycle of simultaneous Read/Write.

It is therefore proposed that the restriction be placed upon the system that the two Exchanges never be allowed to work into the same blocks of memory concurrently. There are several methods which can be used to accomplish this, which ever is most suitable from an engineering and performance standpoint. The allocation of the blocks of memory does not need to be permanent but can be changed after the Exchanges have completed the transfer of information between the designated blocks of memory and their respective I/O units. In this case either Exchange would have priority in access to the requested memory and conflicts could not occur. The presently proposed bus system would be satisfactory.

If we do not allow this restriction there are two alternatives. Either the word rates of the High Performance Tapes and Disks be reduced or a large degree of buffering, timing and control must be added to either the Basic or High Speed Exchange, which, if it can accomplish the objectives, will be very costly.

It should be pointed out also, that the timings for the High Speed Exchange do not include provision for grouping and distribution (scatter read-scatter write). With the provision included for allocation of memory blocks to the two Exchanges the resultant time for word transfers in the worst case would turn out to be of the order of 14.7 usecs for a simultaneous Read/Write cycle and in the best case 6.6 usecs. Thus it can be seen that to include the provision for grouping and distribution the word rate of the High Speed units would have to be reduced.

Another factor which has not been mentioned but which seriously affects input/output performance is the proposed inclusion of the Hamming checker on the input/output bus. Referring to Stretch File Memo #61

the access time when obtaining a word from memory in the worst case increases from 4.5 to 6.0 usecs and when storing a word increases the access time to 3.0 usecs. Without considering a conflict from the Basic Exchange in gaining access to a memory the word transfer time for a simultaneous Read/Write cycle for the High Speed Exchange is now 9.0 usecs in the worst case. With the Hamming checker on the bus, either the word rate of the High Performance Tape and Disks must be reduced or the computer must be prevented from gaining access to memory during the time that the High Speed Exchange is operating in simultaneous Read/Write together with the provision that the two Exchanges are not allowed to operate concurrently with the same memory block.

CONCLUSIONS

The design of the system will include the provision that separate memory blocks be allocated to the two Exchanges during their periods of operation so there can be no possible conflict between the two Exchanges in gaining access to a memory. This implies no restriction on the computer gaining access to a memory, other than that already imposed by either Exchange having top priority. It should not be inferred that permanent allocation of memory areas to the two Exchanges be made unless this can be proven necessary and desirable from an engineering and performance standpoint.

The second conclusion is that the High Speed Exchange will not include provision for grouping and distribution unless a decision is reached to decrease the word rate of the high performance units.

The third conclusion is that the ECC Checker and generator cannot be on the memory bus. Further investigation of what should be done about incorporating these checkers and generators into the system is necessary.

Comments from interested parties on the subject of this memo are requested.