cap. 32 adapters (med. speed units)
64 low speed devices (8 ms/bits)
Weights: 729 III - 4 (15-30 μsec/bits)
729 II - 2 (30-60 μsec bits)
729 I, C.R., C.P., Pr - 1 (60+ μsec bits)
Total weight = 32

COMPANY CONFIDENTIAL

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EXCHANGE MEMO NO. 18

SUBJECT: Switching Between The Exchange And The Input-Output Units

BY: R. P. Fletcher

REFERENCE: Exchange Memos 8, 15, 16

The magnetic core crosspoint switch will not be used in the Exchange. A transistor multiplexing switch is used in place of the crosspoint switch. The transistor switching method has the following advantages over the crosspoint switch:

1. Standard circuits are used.
2. Less transistors are required, resulting in greater economy and reliability.
3. Transistor switching is more modular.
4. Fault location is easier because information from or to an input-output unit always goes through the same circuits.
5. Transistor switching provides D. C. signals between the Exchange and input-output units, allowing for easier compatibility between I/O

units used with both the 700 series and 7000 series systems.

6. More simultaneous operation is obtained by:

   a) Assigning the lower addresses to the higher speed I/O units. This is true because the I/O scanner (called channel scanner in previous memos) has a built in priority in that it scans in sequence from unit 0 to unit 31.

   b) Weighting the I/O units according to their speeds.

A counter is stepped plus when a unit is started and minus when a unit is stopped. If the counter reaches a predetermined value no more units are started. For example, the counter is stepped plus 1 if a slow unit is started; if a faster unit is started the counter is stepped plus 4. This scheme allows for the number of I/O units operating simultaneously to vary according to the speed of the I/O units. The number of I/O units that may be operating simultaneously is no longer limited by the speed of the fastest unit connected to the Exchange.

Figure 1 shows Exchange information flow and Figure 2 the switching required for each I/O unit connected to the Exchange. The gating in Figure 2 is controlled by the I/O scanner and the I/O decoder. The I/O scanner has an output (gate I/O unit) associated with each I/O unit and an input (service request) from each I/O unit.

The I/O unit generates a service request signal each time it has a byte to send into the Exchange (reading). This signal turns on the service request trigger associated with the I/O unit. The I/O scanner signals the Exchange to dwell on this unit for a 1 usec byte cycle. The cycle for this particular I/O unit may not occur immediately but it will take place before the unit is ready to send the next byte.

When the Exchange does dwell on this unit for a 1 usec byte cycle, the unit's associated gate line from the I/O scanner is conditioned, opening the gate between the I/O unit and the Exchange. The other 31 gate lines from the I/O scanner are deconditioned during this cycle. The I/O unit's gate line is also encoded to make a binary address. This address is used to read the unit's data word from Exchange memory. For example, if the Exchange executes a byte cycle for unit 5, then the line "gate I/O unit 5" from the I/O scanner is conditioned, causing data word 5 to be read from Exchange memory and opening the gate between I/O unit 5 and the Exchange. The data word read from Exchange memory is shifted left 8 bit positions and the 8 bit byte from unit 5 is added to the data word and written back into Exchange memory.

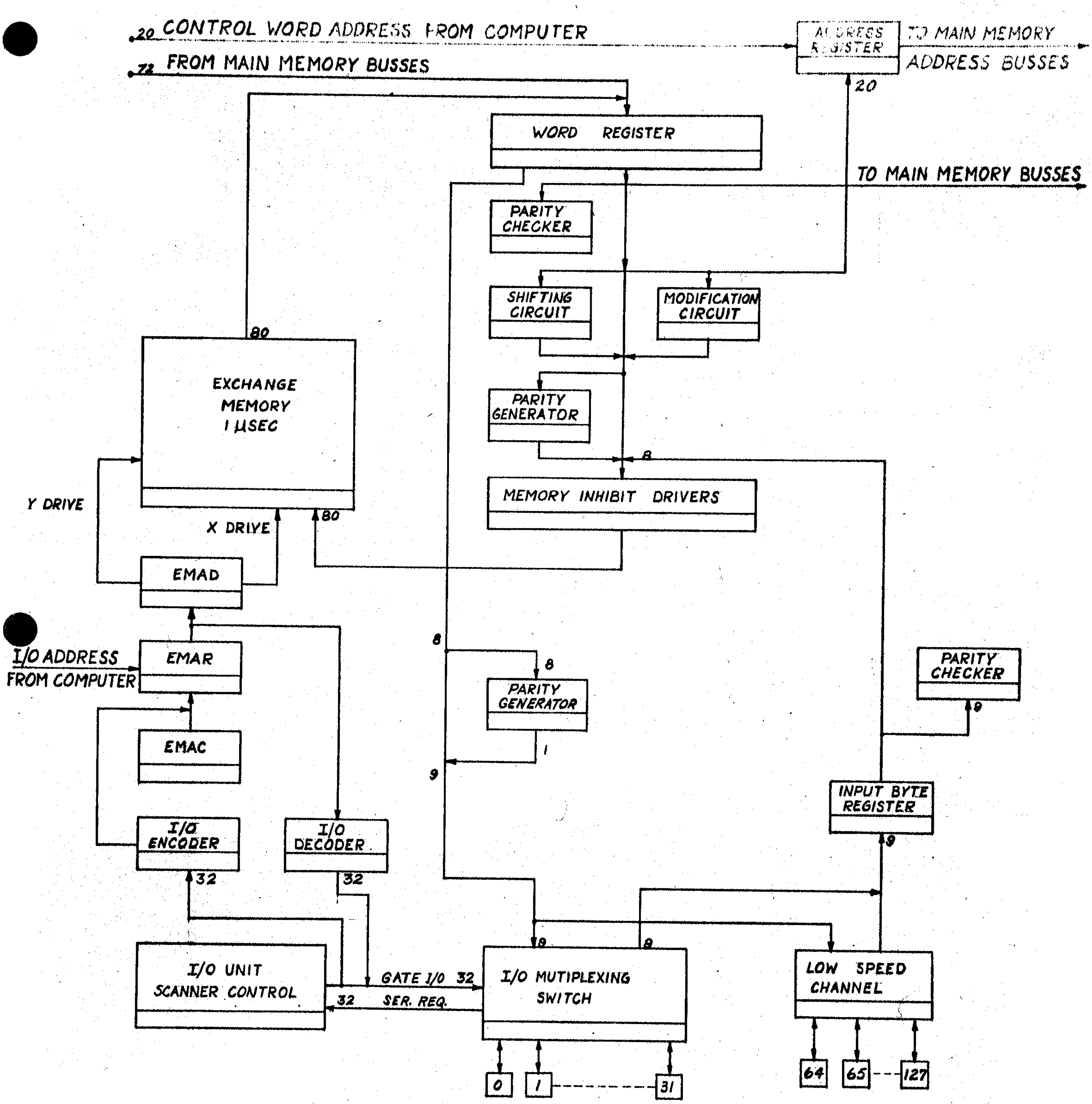
If an I/O unit is writing it generates a service request signal each time it writes a byte. The I/O scanner signals the Exchange to dwell on this unit for a 1 usec byte cycle. The I/O unit's gate line from the I/O scanner is encoded to obtain the address of the unit's data word. The data word is read from Exchange memory. During this cycle the unit's gate line is conditioned and the left 8 bits (and a parity bit) are set into the unit's associated trigger register. The byte is now available to be written by the I/O unit. When the unit writes this byte it will send a service request into the Exchange and the above operation is repeated.

When the Exchange receives an instruction for an I/O unit, the unit's address is set into EMAR and its control word is read from Exchange memory. During this same cycle the I/O address in EMAR is decoded. The 32 outputs of the I/O decoder are ORed with the outputs of the I/O scanner.

For example, if an instruction is received for I/O unit 7, address 7 is set into EMAR and the 7 line from the I/O decoder is conditioned. The 7 line from the I/O decoder is ORed with the gate I/O unit 7 line from the I/O scanner, opening the gate between unit 7 and the Exchange.

This permits the Exchange control circuits to look at the I/O status lines (not ready, etc.) coming from unit 7 and make a decision as to whether the Exchange should accept or reject the instruction.

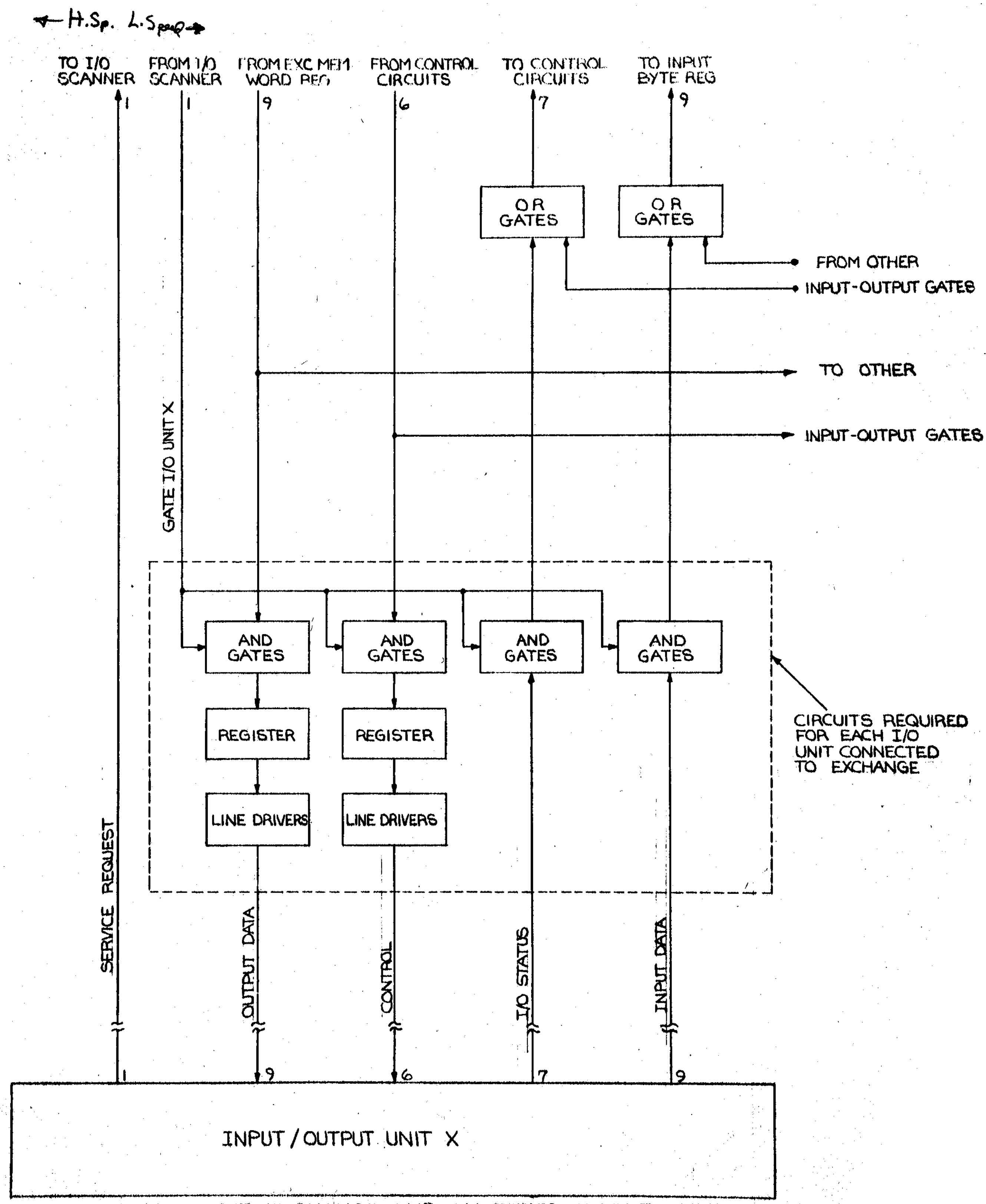
The outputs of the I/O decoder are also used when a unit is started or disconnected. At the time a unit is started or disconnected, its address is in EMAR. The Exchange control circuits generate the proper signal and the I/O decoder gates the signal to the unit whose address is in EMAR. The signal turns on a trigger associated with the I/O unit and the trigger supplies a D. C. control signal to the I/O unit.



INFORMATION FLOW OF EXCHANGE

FIGURE 1

X change memory
1 word for control wd storage
2 words for Data Storage



GATING · BETWEEN · THE · EXCHANGE · AND · AN · INPUT – OUTPUT · UNIT

FIGURE 2