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PROJECT STRETCH
LINK COMPUTER MEMO NO. 6

Subject: Adding One to Memory

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The following is a scheme for partitioning memory into cells of sizes which are powers of two for the ADDing, ORing, or ANDing of a one into any cell in memory. (This concept can be extended to include inserting more than a single bit of information.)

The normal operation for the byte position in the control of the C register will specify the location within the C register into which the data from the Logic Unit will be assimulated. For example, if the data from the Logic Unit is to form an address such that a count of one is to occur in any one of eight cells in any one of 2^7 words, 10 bits of data must be supplied by the Logic Unit, together with a prefix from some source, to form the word and byte address where the one will be counted. The number of cells in each word can be controlled by the position in the word and byte address in which the 10 bits are formed. For this example, the initial byte assembling position control would be loaded with 000011 causing the 10 bits to be assembled in bits 4 through 13 and causing zeros to occur at all other bit positions. (The bit positions are numbered starting with zero.)

The byte address formed under control of the previous word need not be communicated to the memory. The new byte address, the address of the one bit to be added, could be used to form a new data word of all zeros except the single bit to be added, and this word would then be added to memory. Since the necessity for decoding the byte address is already imposed on the C register's control, it seems reasonable to impose the forming and storing of the new data word on the C register control

The memory alerted by the address would be told whether the cycle would be a read or a write. In addition, it would have to be told whether or not the write was a STORE, an OR, an AND or an ADD ONE to memory.

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