September 20, 1956

PROJECT STRETCH

LINK COMPUTER MEMO NO. 5

SUBJECT: Data Register Organization
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A system of registers is defined along with their controls, capacities, and characteristics. Various techniques of using the register organization are described to prove the versatility of the system.

The proposed data register organization for the Link Computer, consists of three full word registers which can be identified by the letters A, B, and C. (see Figure 1). Associated with each register, is a read out core shift matrix, and associated with registers B and C is a read in core shift matrix. (For reference to core shift matrix operation, see Link Computer Memo No. 4). All three registers can receive from and send to memory (through respective buffer registers) any of the following:

a) A full word
b) A half word low order bits (right)
c) A half word high order bits (left)
d) Split words or selective bits can be transferred by a masking control between the data registers and the buffer registers (not shown in Figure 1).

The arithmetic use of the registers may help to specifically identify them.

Register	Before Execution	After Execution
A	addend	addend
B	augend	augend
B *	augend	sum
C	------	sum
A	multiplicand	multiplicand
B	multiplier	product (high)
C	----------	product (low)
A	divisor	divisor
B	dividend (high)	quotient
C	dividend (low)	remainder

* Alternative possibility for use of Register B in which case Register C would not be involved in addition or subtraction operations.

Register Controls

Each register has associated with it a complement of control equipment. The characteristics of the unique control features, are identified and discussed. (See Figure 1, Register Controls).

Byte Size Control

A byte size control is associated with each register which indicates and controls the increment number of bits to be taken from the associated register for any given processing cycle. (The data entity is taken out through the core shift matrix). The byte size also controls the increment between successive core shift matrix diagonal pulsing which releases the data for processing. Normally, the byte size control associated with a register will remain set a any given byte size until set to a new value.

Word Address Register

The entity presently named the word address register, has the capacity of remembering where the word came from that is presently stored in its associated data register. The word address need not be a full address, but may conform to the block address scheme generally considered advisable to reduce the required number of bits to represent a specific memory location. A left half, right half, and both halves identification is included to help insure uninterrupted operation during a continuous flow execution. In a continuous flow type of operation, the register will initially be filled with both halves of the specified word of data. As the bytes of the word are removed for processing, the number of remaining bytes is reduced. When half or less than half of the data word remains unused, preparations are made automatically to step up the address in the Word Address register, initiate a memory access to get the next data word and finally, store the right half of the new data word in the register area that originally contained the data that was first involved in actual processing. A subsequent cycle would replace the old left half word and may or may not require an additional memory reference. The word address register contents are stepped only after both halves of a data word have been used, and then only if the computer is in a continuous flow type of operation. Provision will have to be made to restore the original or starting address if it will be possible to advance more than one word length beyond the starting point and then automatically recycle to the starting word.

Field Length Counter

The field length counter has as its main purpose, the defining and limiting control on the number of bytes (or number of cycles in certain cases) to be involved in a specific type of execution. A Starting Point Field Length register feeds the actual field length counter so that snap back, or recycling actions can be provided for. (e. g. in the case of recomplementing or in a stream of successions type of operation).

Bit Address Counter

The bit address counter specifies the particular bit in a given word where the first byte for processing is to be found. The Starting Point Bit Address register feeds the initial bit starting point to the bit address counter, which at all times, identifies the first bit of the next byte to be used in processing. Thus, provision is made to, at all times, identify the starting bit and to identify the first bit of the next byte to be processed. The Starting Point Bit Address register has the ability to be advanced, thereby re-defining the starting point on subsequent process cycles fulfilling the requirement of a Stream of Successions type of operation. The advancing of the starting point should be restricted to the limits of byte size.

Capacities:

The capacities of the various control elements are still unsettled, but an attempt will be made here to list what is presently felt as reasonable quantities. The basic data word size and individual register length is 64 bits. The Byte size should be permitted to vary from one to eight bits.

The Word Address Register should be within the limits of a block definition (perhaps 12 bits) at the greatest, its capacity cannot exceed 20 bits.

The Field Length Counter for all practical, scientific and commercial applications, should be limited to a value of 128 (7 bits), thereby permitting an excursion through two complete words with the smallest size byte (1 bit). The special case of streaming will have to be studied to determine a reasonable field length limit.

The starting point bit address, since it must be capable of identifying any one of 64 bits in a word, must have a capacity of 6 bits. If the starting point is advanced, then a starting point "wrap around" will automatically increment the Word Address Register or in the specially identified case, the incrementing would be done to the Starting Point Word Address. The Advance mechanism will be capable of incrementing the Starting Point Bit Address by the size of a byte, which may vary from one to eight bits.

Various techniques of using the data register and control system organization have been indicated in the actual definition. An area as yet unmentioned will illustrate the extreme flexibility of the proposed system. Since each register has independent controls, it is, therefore, possible to conceive operations which specify Add an eight bit byte from Register A to a six bit byte in Register B, and deposit the sum as a four bit byte in Register C. Since the registers are basically independent, data words can be automatically and independently obtained from memory, and resulting words can likewise be stored in memory.

Many areas still remain to be investigated, however, preliminary problem analysis indicates the necessity for an extremely flexible data manipulating system such as the one herein described.

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WW:gmp

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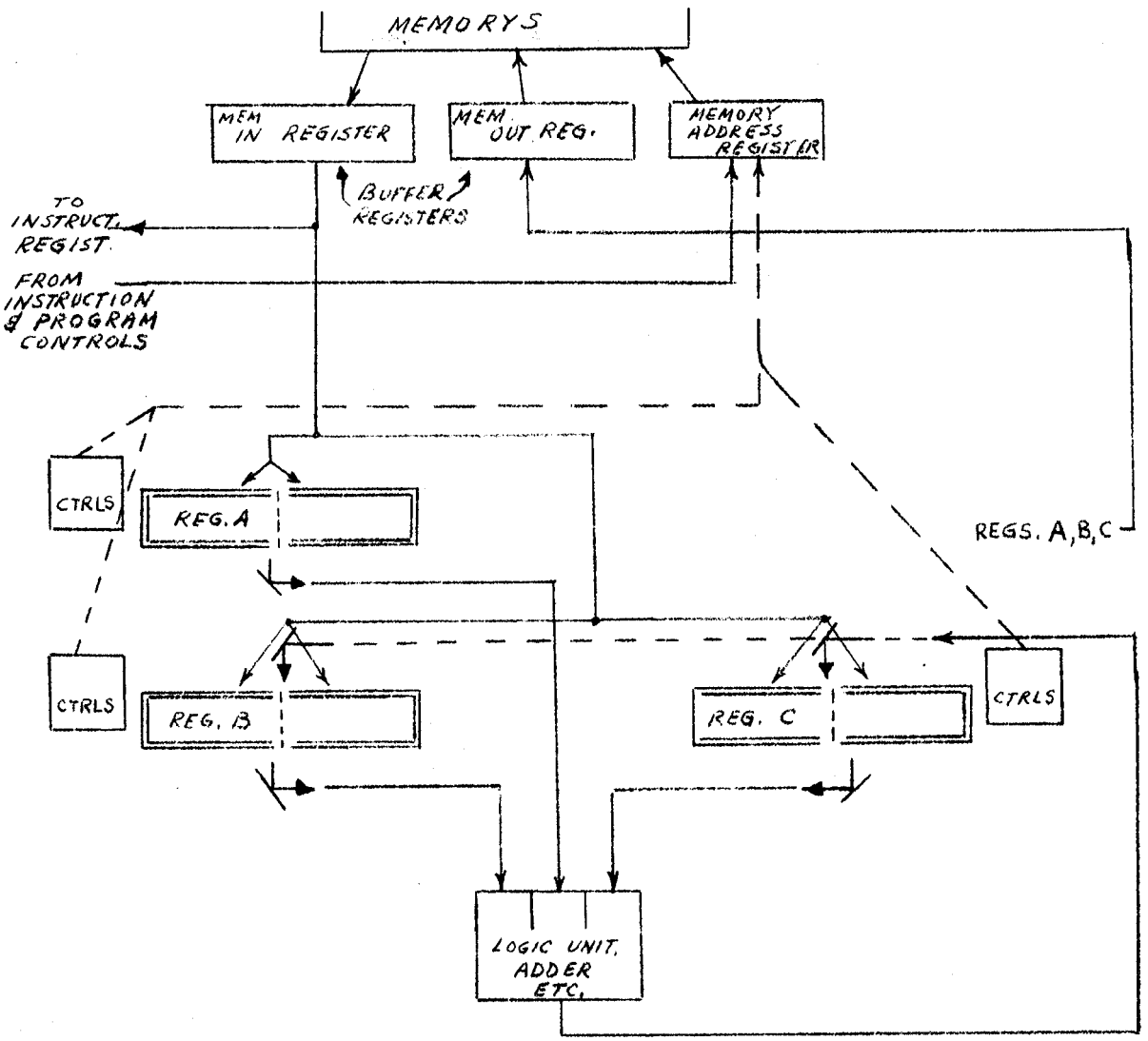

LINK REGISTER ORGANIZATION

REGISTER CONTROLS

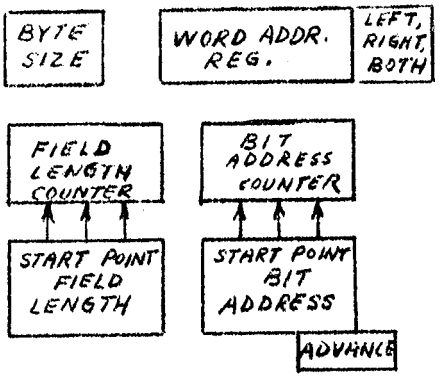

fig. 1

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WW