COMPANY CONFIDENTIAL

Griffith

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Exchange Memo No. 13

A Proposed Block Diagram for Exclusive OR and Flip-Flops

By: Frank Tung

The block diagram representation of the logical Circuits considered in Exchange Memo No. 6 are extended to cover the EXCLUSIVE OR CIRCUITS and the Flip-Flops. They are an attempt to present one of the many forms of suitable block diagrams of those circuits. The characteristic of the block diagrams are conformed to those presented in Exchange Memo No. 6. All the component circuits to be mentioned are developed by the Transistor Circuit Group.

For the sake of convenience, the definition given in Exchange Memo No. 6 is repeated. The system is composed of two types of transistors -- PNP or NPN.

1. The output of the P blocks (made of PNP transistors) are designated with a subscript p and the output of the N blocks (made of NPN transistors) are designated with a subscript n.
2. The outputs of P blocks (p lines) can be used only to drive N blocks, whereas the output of N blocks (n lines) can be used only to drive P blocks.
3. Signal on the n line is a 1 if it is in its most negative voltage and signal on the p line is a 1 if it is in the most positive voltage.
4. By inserting a level Setter as part of the load, it is possible to construct logical connectives, the input and output lines of which have the same characteristics.

I. EXCLUSIVE OR CIRCUITS

An EXCLUSIVE OR CIRCUIT can always be formed by combining two AND CIRCUITS and an OR CIRCUIT. However, 9 transistors will be required if it is combined in the above manner. The Transistor Circuit Group has developed an EXCLUSIVE OR CIRCUIT which is composed of

either 6 transistors or 4 transistors. The 4 transistor EXCLUSIVE OR CIRCUIT offers no complemented output. One of the applications where an EXCLUSIVE OR connective would prove extremely useful in the Exchange lies in the operation of stepping the word count -1 and the Data word address +1. By using an EXCLUSIVE OR and an AND connectives for each bit, the carry propagation time is determined solely by the number of parallel blocks that can be cascaded at an output of a logical connective and the number of parallel inputs that a logical connective can handle.

a. The circuit and the corresponding block diagram of a 6 PNP transistor EXCLUSIVE OR connective with complemented outputs are shown in Figure 1. By reversing the subscripts, the same block diagram can be used for the NPN version of the same circuit.

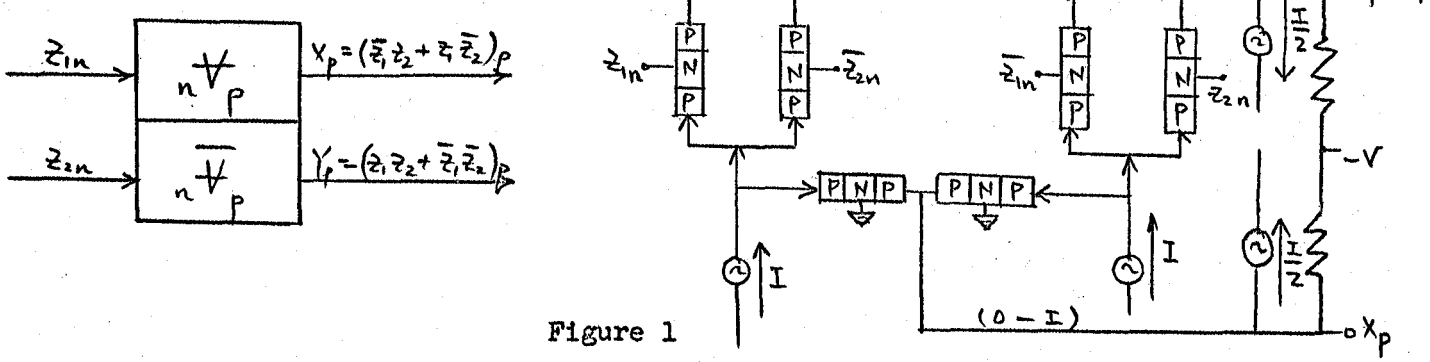

Figure 1

Only two lines are shown leading to the input of the block. The actual circuit involves the connection up to four inputs -- the two signals and the complements of each signal.

A block diagram that may be used to represent a 4 transistor EXCLUSIVE OR connective which has no complementary outputs is shown in Figure 2. The actual circuits has only two inputs as those shown.

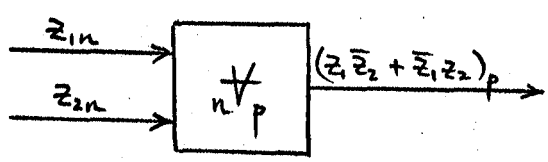

Figure 2

The saving of the two transistors is at the expanse of adding 4 diodes and two current sources. Each current source supplies the amount equals to the d.c. current of the conducting transistor.

II. FLIP-FLOPS

A. Standard Flip-Flops

The state of the standard Flip-Flop is determined by the application of a pulse at either the Set or Reset terminals. The polarity of the pulse depends on the type of transistors that made up the Flip-Flop. The input terminals are normally at the voltage which corresponds to a zero for the particular line. For instance, the input signal will be at it's most positive voltage if it is an n line. In order to trigger the Flip-Flop the input signal is changed to its 1 state. Depending on the type of input lines, this change may appear either as a positive or a negative pulse.

Two different types of Standard Flip-Flops will be considered.

1. Flip-Flop composed of both NPN and PNP type transistors.
2. Flip-Flop composed of either the NPN or the PNP type transistors.

1. Figure 3 shows the circuit configuration and the block diagram representation of a standard Flip-Flop incorporating both type of transistors.

The features of this circuit and the notations are explained as follows:

a. The basic circuit with no input trigger circuits requires 4 transistors.

b. It has both types of outputs (p line and n lines) and their complements.

c. K is the number of parallel input transistors shown dotted in Figure 3. The maximum possible number of K is to be determined by the Circuit Group. The parallel connection of those input transistors serves as an OR function. K is redundant since it is specified by the number of incoming arrows. However, it may simplify the

packaging problem if the Flip-Flops are to be mass produced as separate pluggable units.

d. The state of the Flip-Flop is conditioned as follows:

1. $D_n = 1$, $D_p = 1$ Upon application of a 1 at either of the K p line inputs (Z_{1p}, ------,Z_{kp})

2. $\overline{D}_n = 1$, $\overline{D}_p = 1$ Upon application of a 1 at either of the K n line inputs (X_{1n}, ------,X_{kn})

e. The complement of the signal is denoted with a bar.

f. The subscript p and n on the output terminals may be removed if it is remembered that the left side gives a p line output and the right side gives a n line output which can be differentrated by the positions of the subscript associated with the initials F.F.

g. The particular arrangement of the block diagram, is that the top left output is a 1 if it is triggered from the left and the top right output is a 1 if it is triggered from the right.

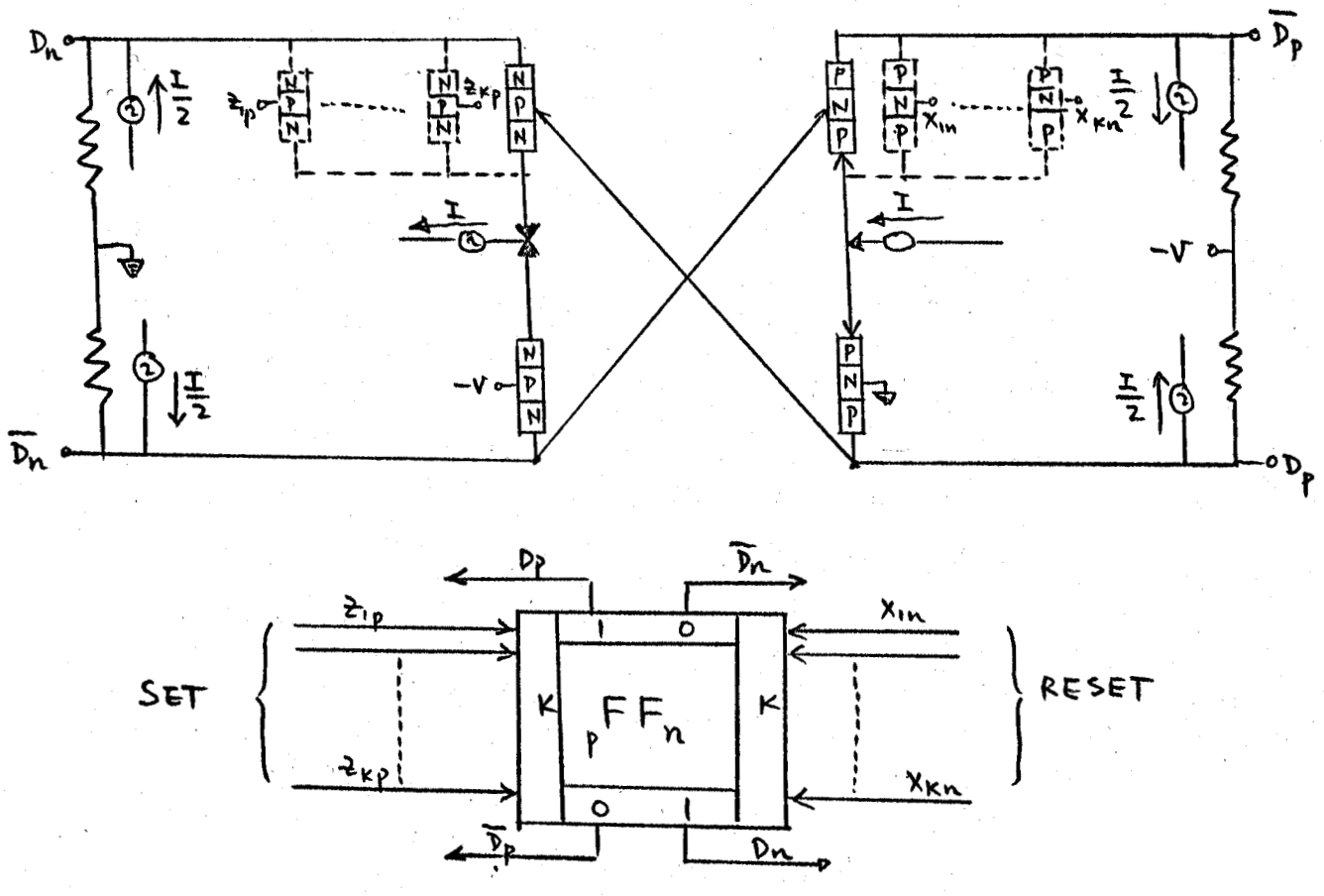

Figure 3

Another block diagram representation of a Standard Flip-Flop whose circuit configuration is shown in Figure 3, has been suggested. It resembles the one just proposed. It is shown in Figure 3a.

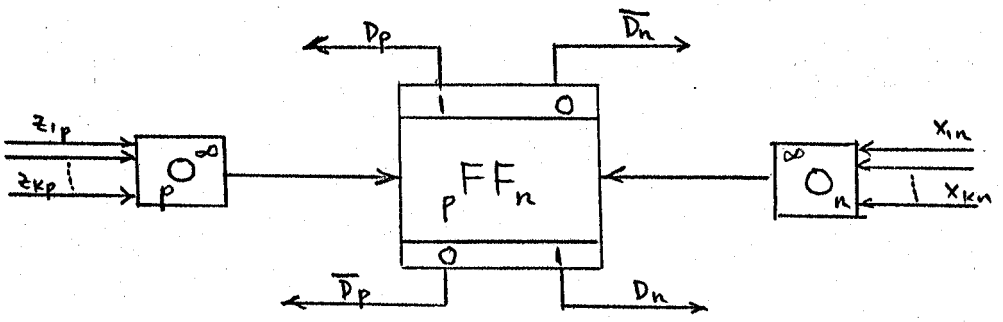

Figure 3a

The form of this representation is such that:

1. The overall block diagram is reduced to three simplified blocks each one of which can be easily grasped.
2. Logic-wise, only one new block is introduced. (The Flip-Flop)
3. The two small blocks perform the function of a OR circuit for the inputs. The ∞ sign signifies that OR block is actually part of the Flip-Flop.
4. The number of inputs is specified by the number of arrows leading into the OR block.

Figure 4 shows the block diagram used by the circuit group of the Exchange to represent a Standard Flip-Flop that has two input terminals -- OFF and ON. P and N stand for the type of transistor used. It is included here for reference.

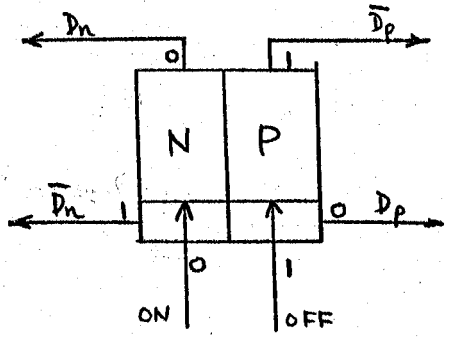

Figure 4

2. The Standard Flip-Flop composed of either the PNP or the NPN type transistors has been developed. It involves the use of selenium diodes and extra power supplies as the level setter at the collector circuit. Both the inputs and the outputs are n lines. The block diagram representation and the component circuit of a Standard Flip-Flop of the PNP type is shown in Figure 5. The state of the Flip-Flop is determined by the application of a negative pulse or a 1 at either one of the many Set or Reset input terminals. K denotes the number of inputs which is the number of transistors connected in parallel as shown dotted. The Flip-Flop itself requires 4 transistors. The input terminals are normally at a voltage which corresponds to a 0.

If a two level logic system is adopted, all the subscripts can be omitted, except one, since the differentration between the n line and the p line is no longer necessary. This subscript is used only to indicate the type of transistor used.

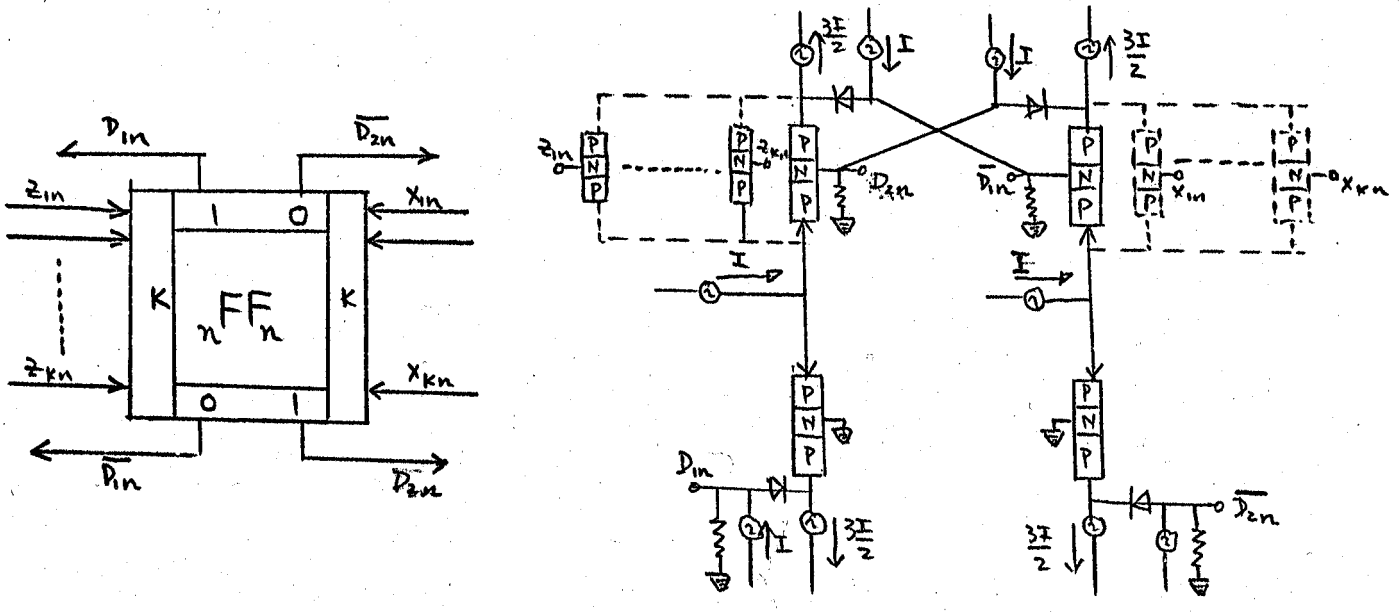

Figure 5

The circuit of Figure 5 also applies to NPN type transistors by reversing the polarities of the selenium rectifiers and the power supplies. It, however, also becomes necessary to reverse the polarities of the input trigger pulses. If the most negative of the two is considered as a 1, it results that a change from a 0 to 1 will be required to

trigger a PNP type Flip-Flop whereas a change from a 1 to 0 will be required to trigger a NPN type Flip-Flop.

II. BINARY FLIP-FLOP

A Binary Flip-Flop changes its state upon the application of a pulse at the binary input terminal. Many binary Flip-Flop Circuits have been developed by the Transistor Circuit Group. New circuits are still being investigated. Like the standard Flip-Flop it is conceivable that a number of transistors may be paralleled as input terminals that perform an OR function. The block diagram of a binary flip-flop made of one type of transistor that has two complementary outputs is shown in Figure 6.

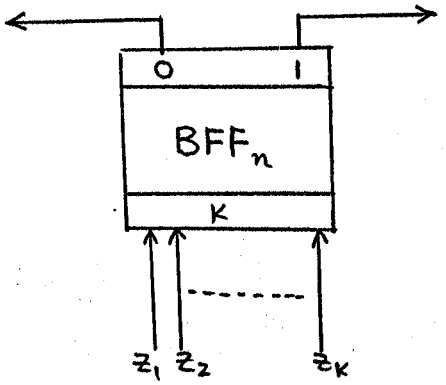

Figure 6

The notation is as follows:

a. BFF stands for binary Flip-Flop.

b. Subscript n stands for the type of transistor (PNP), the type of input lines (n line) and the type of output lines (n lines.)

c. K denotes the number of inputs. Each one of which may be used to trigger the Flip-Flop.

III. CONCLUSION

Certain logical consequence can be inferred from the study of the block diagram

representation with respect to the many developed circuits. Some of the obvious points which deserve consideration are as follows:

1. The degree of complication introduced by a four level logic in a large system.
2. The accessibility of both type of transistors.
3. The reliability of the selenium rectifiers.
4. By using both type of transistors and two level logic, the advantages are:

    a. Block diagram-wise the symbols shown going into a block are the actual wiring lay out.

    b. No restriction on the type of transistors to be cascaded.

    c. Complemented outputs are not essential. Therefore, only one selenium rectifier is necessary per logical block.

Whereas the disadvantages are:

    a. A saving of transistors may be derived from using a four level logic.

    b. Extra power supplies are necessary for the Level Setter. To be specific, at the present operating point of the Junction Alloy Transistor (4 ma) an extra 8 ma at about 40 volts is necessary per output terminal.

The choice of adopting a standard number of circuits for the computer depends upon many other factors. No evaluation has been attempted here. The decision should be reached from the basis which can best be arrived at from an extensive study of laying out a complicated overall logical system, using different types of block diagrams. After a decision is made, the notation of the block diagram may further be simplified. Some redundant subscripts may not be necessary. Efforts will be spent toward this direction.