COMPANY CONFIDENTIAL

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Link Exchange Memo No. 6

Block Diagram Representation of Component Circuits

All component circuits have been developed by R. Henle's circuit group. Information pertaining to various circuits was obtained from E. Slobodzinski, H. Yourke, and P. Halpern.

This paper is concerned with the application of the building blocks currently being developed by the Transistor Circuit group. By defining a proper set of rules for their interconnections, it is possible to lay out a complicated logical system and be able to trace the signal at arbitrary points in the system. The basic building blocks in a computing system are: Amplifier, Flip-Flop, and the logical blocks such as AND, OR, INVERTER, and possibly EXCLUSIVE OR circuits. Only the AND, OR and INVERTER circuits are considered here, and no evaluation is made on the different type of circuits.

The different building blocks are composed of transistors of either PNP or NPN type. The following properties are observed.

1). The signals that appear at the output of the two types of blocks are differentiated by subscripts. The outputs of the P blocks (made of PNP transistors) are designated with a subscript p and the outputs of the N blocks (made of NPN transistors) are designated with a subscript n.

2). The outputs of P blocks (p lines) can be used only to drive N blocks, whereas the outputs of N blocks (n lines) can be used only to drive P blocks.

3). With small voltage signals, the transistor is kept out of the saturation region. The differential voltage between a 1 and 0 is about 1.2 volts.

4). The signal level used are: $\overset{1}{-}\ 0.6$ or $\overset{0}{+}\ 0.6$ volts on the n line and $\overset{1}{-}\ 2.4$ or $\overset{0}{-}\ 3.6$ volts on the p line.

5). Only two out of the four alternative definitions that associate the 1's and 0's with the voltage levels on both the p and n lines will give the same logical statement for both types of building blocks. They are:

a). Signal on the n line is a 1 if it is in its most negative voltage, and signal on the p line is a 1 if it is in the most positive voltage.

b). Signal on the n line is a 1 if it is in its most positive voltage and signal on the p line is a 1 if it is in its most negative voltage.

Either of the two definitions can be used if it is used consistently throughout the system. Definition (a) will be used.

6). Signal on the line are represented by symbols:

Zn refers to signal on n line.

Zn = 1 corresponds to - 0.6V

$\overline{Zn}$ = 0 corresponds to + 0.6V

Zp refers to signal on p line.

Zp = 1 corresponds to -2.4V

$\overline{Zp}$ = 0 corresponds to - 3.6V

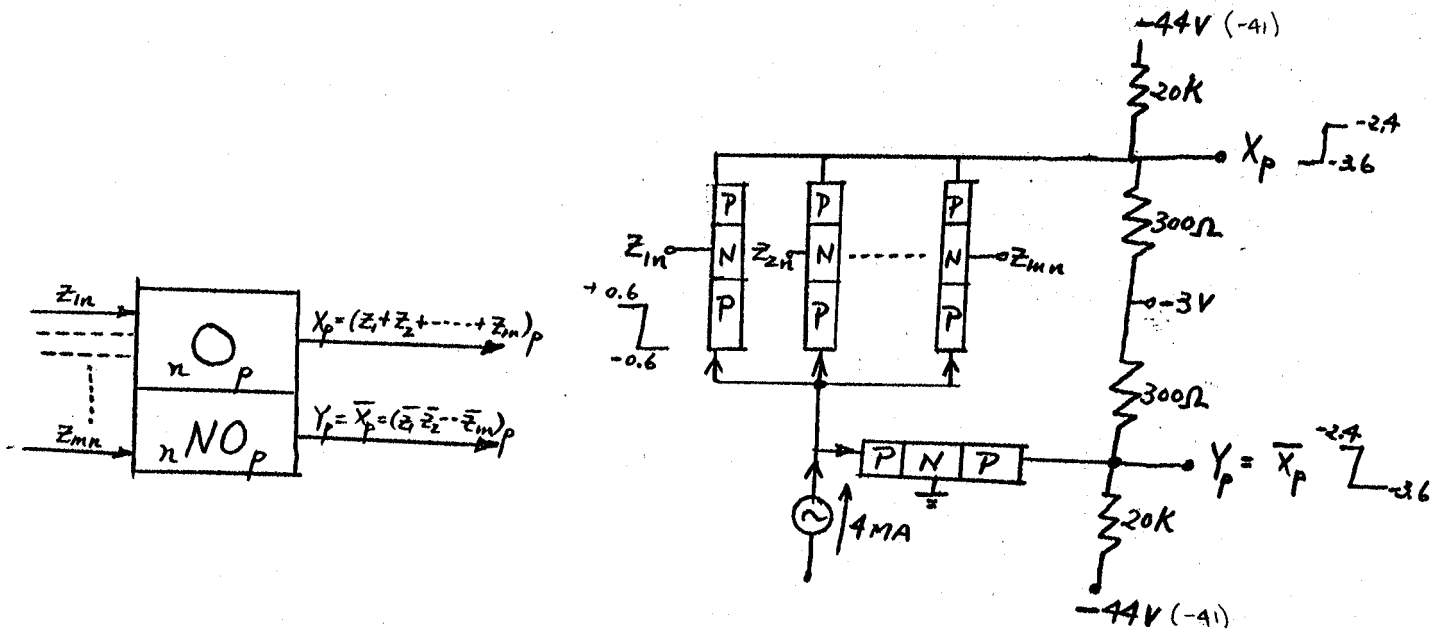


Figure (1)

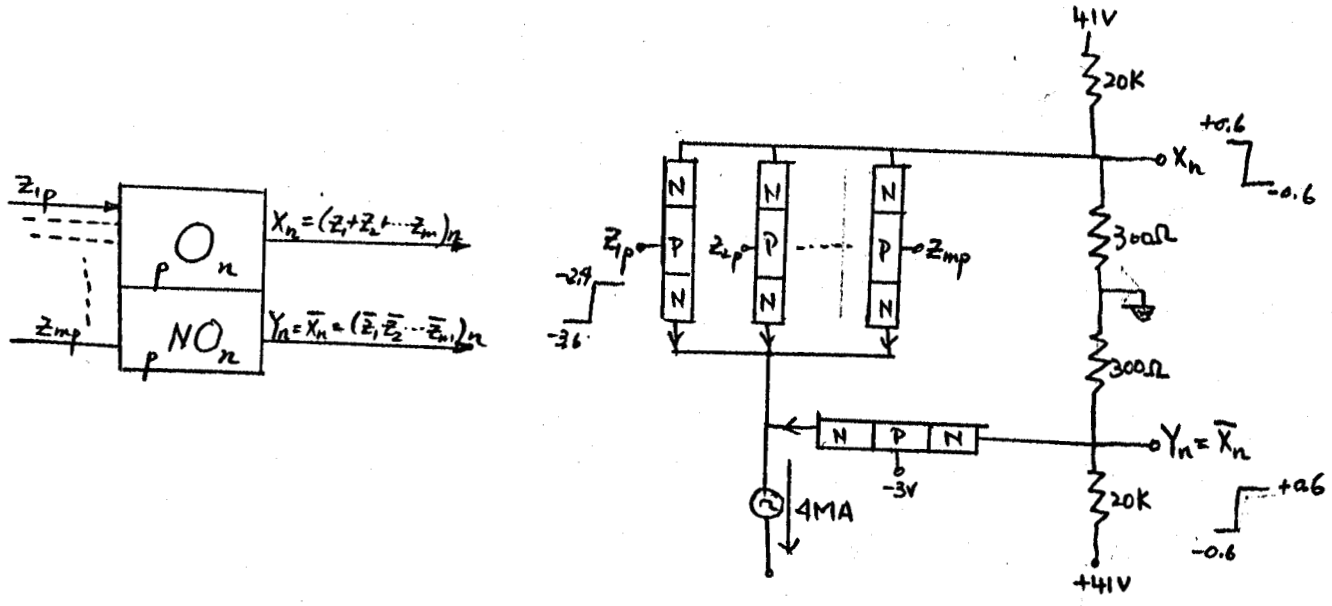
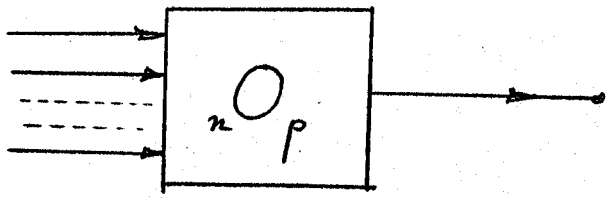


Figure (2)

Figure (1) shows the block diagram representation and the actual circuit of an "M complemental OR circuit" made of the PNP transistors. The NPN version of the same circuit is shown in Figure (2). The subscript preceeding the character in the block refers to the type of input. The subscript following the character refers to the type of output

and the type of transistor that make up this block. The following diagram



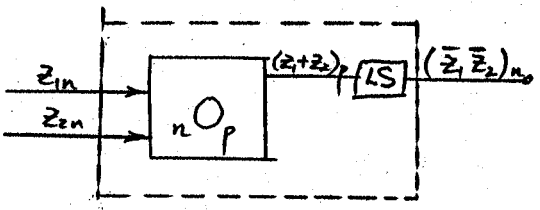
illustrates an OR circuit made of PNP transistors with n lines input and p lines output. The first subscript will always be an n for PNP type building blocks in this system.

Unlike the conventional logical building blocks, this type of circuit provides two outputs which are complements. It can be seen that the OR circuit can also be used as an AND circuit if it is fed by the separate complements of the input signals. The Inverter Circuit is a degenerated OR circuit with only one input. Furthermore, the Inverter Circuit can also be considered as a Converter which converts from a p line to an n line.

In order to avoid the confusion between p lines and n lines, it may be desirable to construct a single logical connective, the input and output lines of which have the same characteristics. A circuit which accomplishes this need has been developed by the Circuit group.

The load circuit of the building blocks shown in Figure (1) and (2) are modified by inserting a selenium rectifier so that the output terminals are complements and can be made to swing between the same voltage levels as the input signals. The PNP version of the circuit and the block diagram representation is shown in Figure 3.

Block Diagramwise, the load circuit of Figure (3) can be considered as a level setter which inverts and in the same time converts the signal from p line to an n line.



It should be noted, however, that $(Z_1 \neq Z_2)$ p is no longer available since LS is part of the load.

By keeping the same definitions concerning the 0's and 1's, four possible circuit configurations can be constructed from PNP transistors. The operational performance of the circuits can be characterized by the following block diagrams. For simplicity, only two inputs are shown.

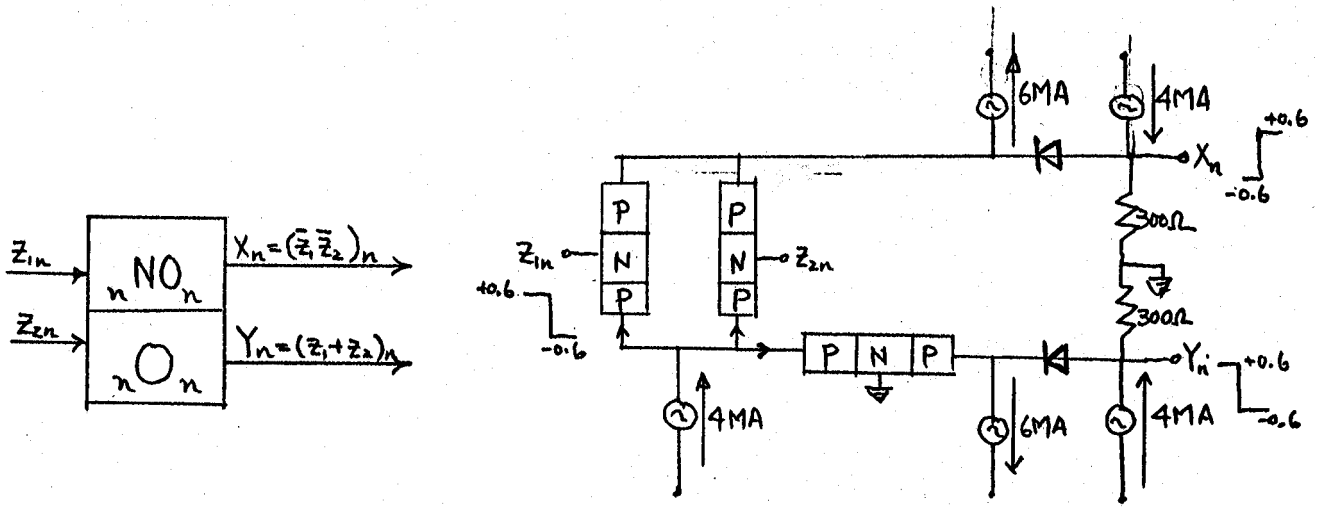
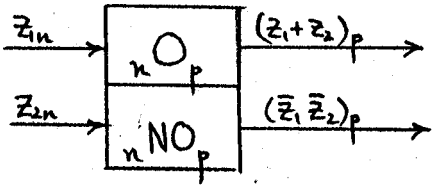
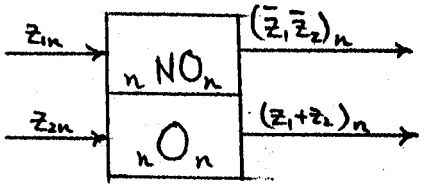


Figure (3)

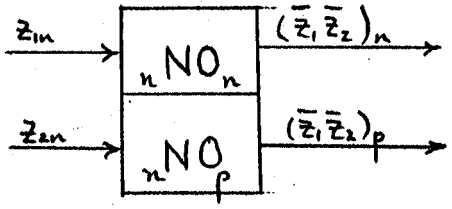
a)



c)



b)



d)

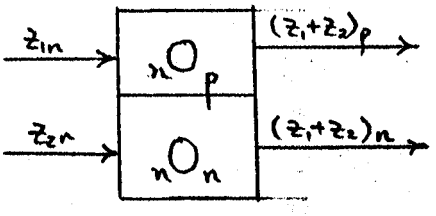


Figure (4)

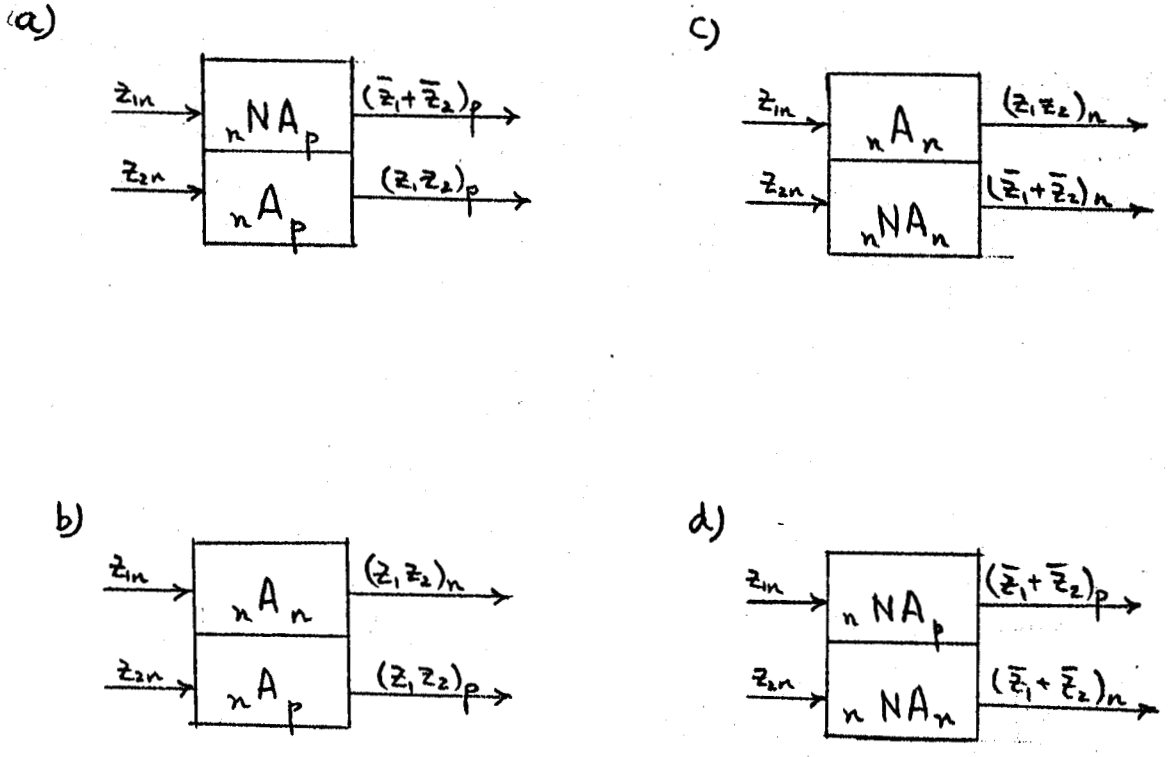


Figure (5)

If all the inputs are complemented $(Z_1, Z_2 \ldots\ldots\ldots Z_{in})$, then the OR circuit performs an AND function. One of the two outputs is $(Z_1, Z_2 \ldots\ldots\ldots Z_{in})$; the other is $(Z_1 \neq Z_2 \neq \ldots\ldots\ldots Z_{in})$. To help visualization, a set of fictious blocks corresponding to OR circuits are defined shown in Figure (5). It is kept in mind, however, that in the

actual layout of the wiring diagram for those AND circuits, the separate complement of these input signals shown should be used. Furthermore, we define an inverter block.

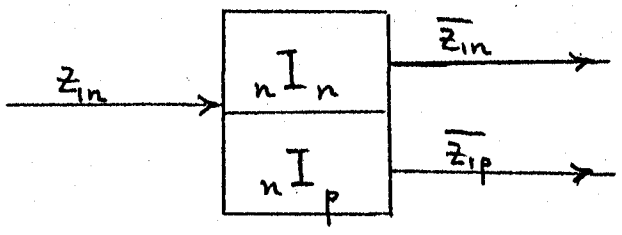


Figure (6)

The inverter circuit is the same as Figure 4b, except the inputs are reduced to one line. Corresponding to blocks shown in Figure 4, 5 and 6, are a set of logical blocks constructed by NPN transistors if all the subscripts between p and n are interchanged.

Only two of the four blocks shown in Figure 4 are necessary to provide the possible outputs. (4a and 4c or 4b and 4d.) The advantages and disadvantages of various circuits are:

Figure 4a

1) This circuit uses no selenium rectifiers and hence is economical.

2) The output is limited to drive only the NPN transistors.

Figure 4b and 4d

1) It is more flexible in that both the p line and n line outputs are available.

2) Each circuit requires only one selenium rectifier.

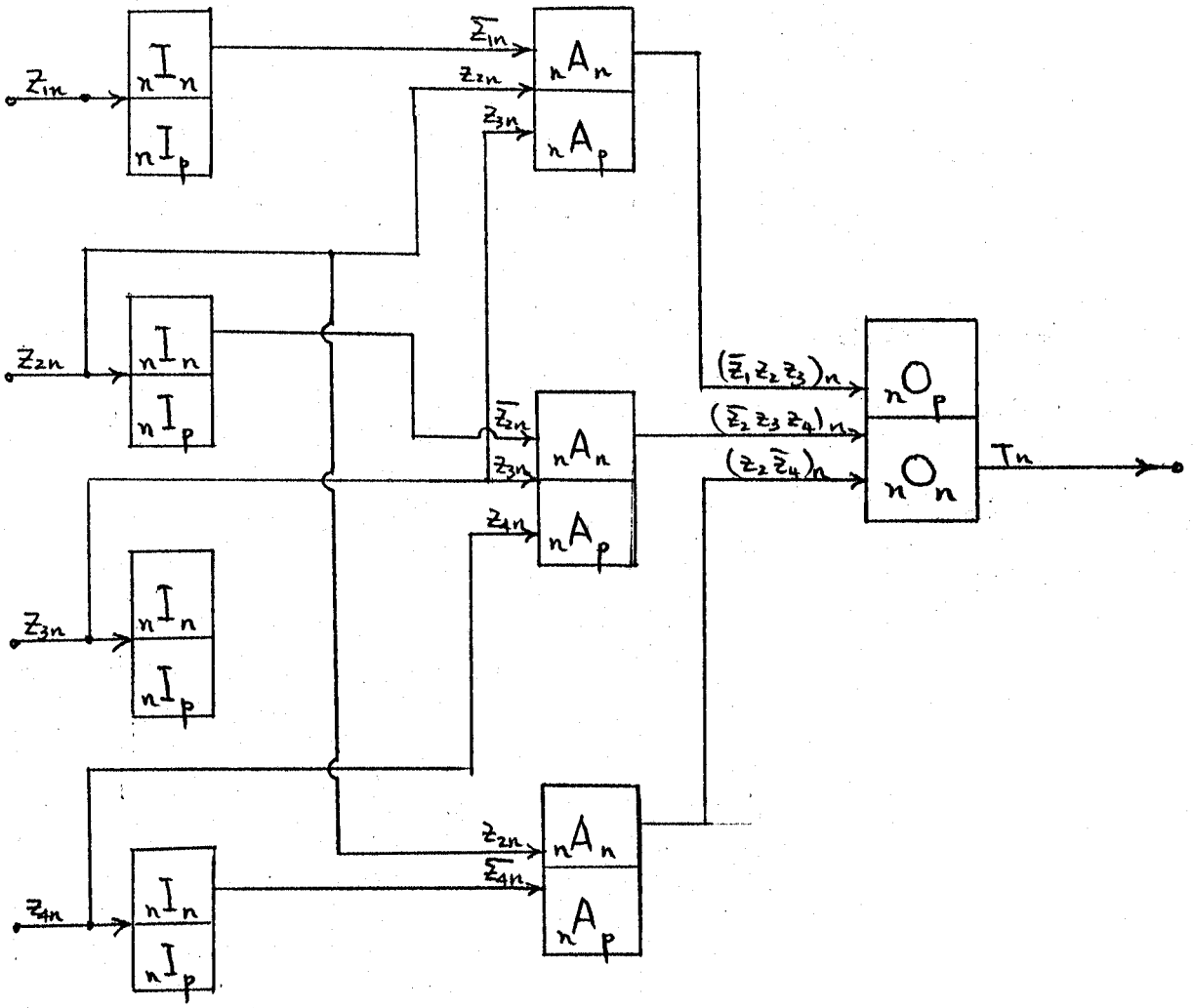
3) It provides an amplifier gain.

Figure 4c

1) This circuit eliminates the confusion between p and n lines at the expense of having two selenium rectifiers.

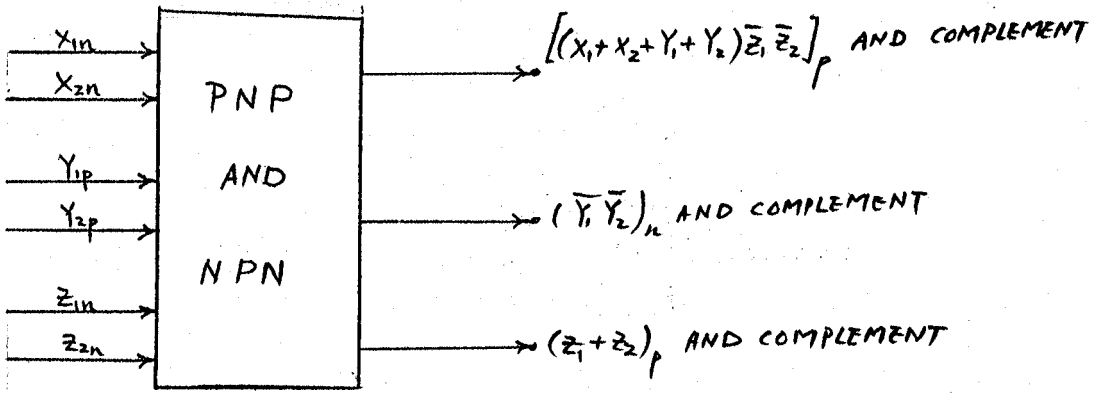
The following is a block diagram of a simple Boolean function in its minimum normal form, using building blocks shown in Figure 4b and d.

$$T = \overline{Z_4}\ Z_2 + Z_3\ Z_4\ \overline{Z_2} + \overline{Z_1}\ Z_3\ Z_2.$$



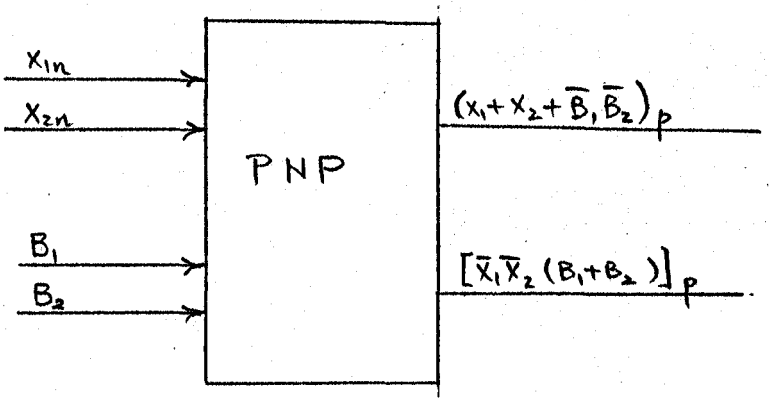
If circuit of Figure 4a is used together with the NPN version of the same circuit, a saving of 8 rectifiers is obtained. Nevertheless, the total number of transistors used remains the same. It is definitely not economical to use the circuit of Figure 4c since only one of the two output terminals are used.

Many other circuits have been developed which can perform logic on input signals that consist of both p and n lines. For example.



In particular logical circuits making use of the split level inputs have been developed. It eliminates one transistor in a simple OR circuit. The disadvantages lie in that it introduces one more voltage level which may be undesirable in the long run.

For instance:



X_n = - 0.6V B = 0V

$\overline{Xn}$ = + 0.6V $\overline{B}$ = 1.2V

With split level input, an Exclusive OR circuit can be constructed with only 4 PNP transistors. The practical use of these circuits have to be further investigated.

One alternate and more uniform representation of building blocks is proposed. The total number of basic building blocks are reduced to three. These are AND's, OR's and INVERTERS.

1) Only two voltage levels + 0.6V and - 0.6V are used throughout the system.

2) It makes use of both type of transistors (PNP and NPN).

3) Different building blocks are made of different types of transistors. OR circuits are constructed by PNP transistors and AND circuits are constructed by NPN transistors. (This is the result of the definition that -0.6V is 1 and ≠ 0.6V is 0).

4) The notations associated with the building blocks are simple.

5) Subscripts denoting the type of lines are no longer necessary.

6) Eliminates a -3V power supply.

7) Unlike the previous case, the AND circuit does not require at its input the separate complements of the input signals.

8) Building blocks can be mass produced as separate units and hence may be more economical.

9) The definition of the signals on the line are $Z = 1$, $\overline{Z} = 0$.

10) The Selenium rectifiers used are of very low cost.

11) If the definition is altered so that -0.6V is 0 and ≠ 0.6V is 1, the AND and OR will be interchanged.

OR functions will be constructed by NPN transistors whereas an AND circuit will be constructed by PNP transistors.

The three types of building blocks and their associated circuit configurations are shown in Figure (1), (2) and (3), respectively. The subscript in the block refers to the type of transistor that made up the block. It is actually redundant since the components are implied by the type of building blocks.

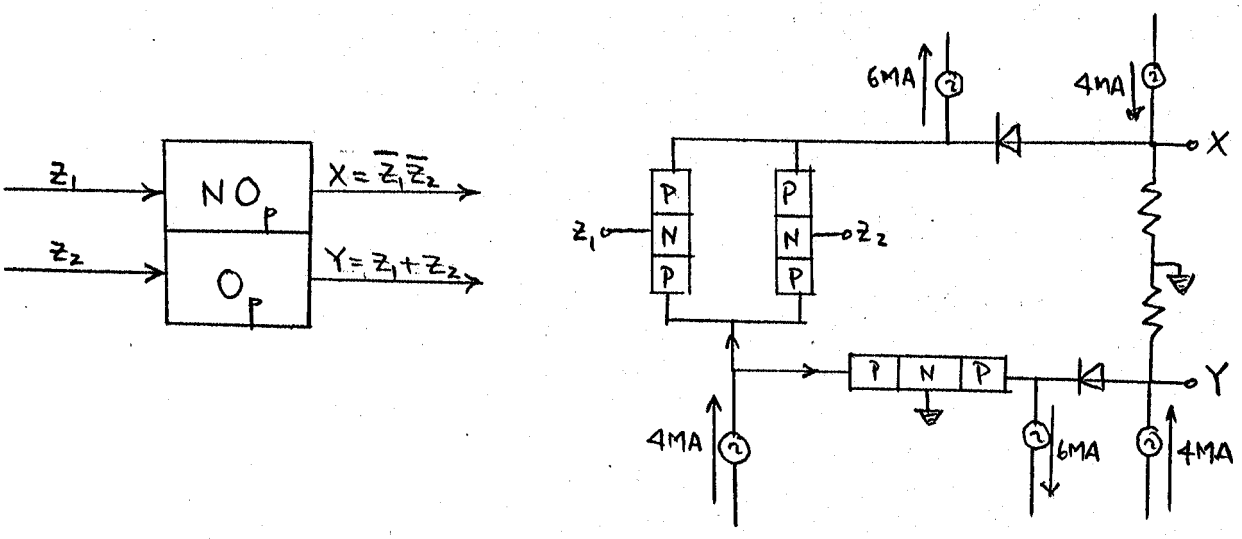


Figure (1)

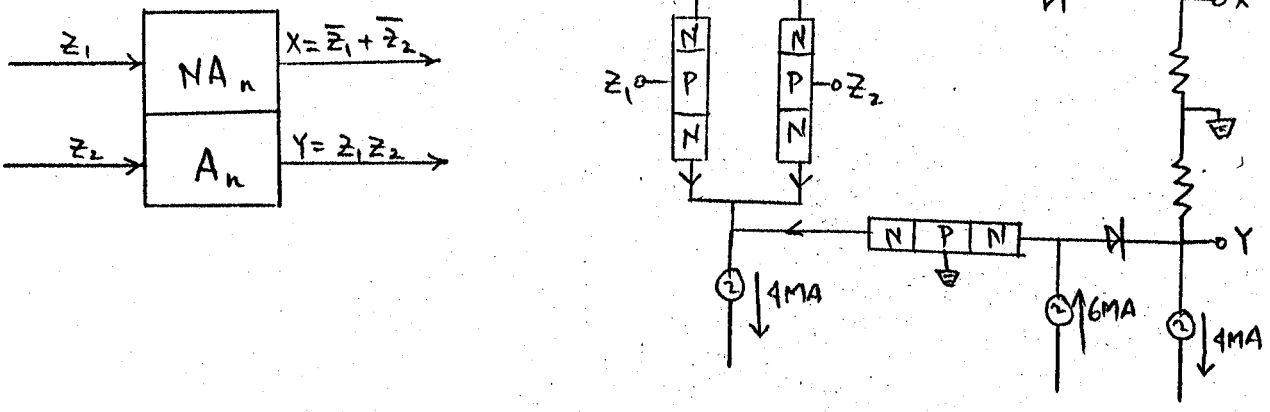


Figure (2)

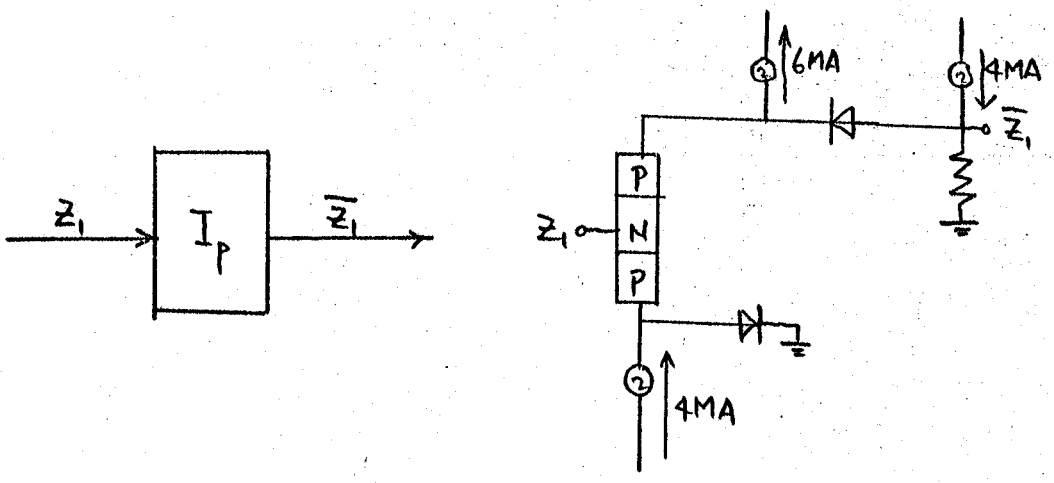


Figure (3)

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