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PROJECT STRETCH
DELTA COMPUTER MEMO NO. 18

Subject: The Indicator Register in the Delta Computer

By: W. Wolensky

The indicator system of the Delta Computer performs a vital function necessary to the basic philosophy of operation of the STRETCH system. Brief, but intensive consideration has been given to the many factors involved in the development of the basic core of the computer's operation. The preliminary conclusions are listed and explained.

The fundamental concepts of the STRETCH system include multiprogramming, flexible break-in, and real-time operations, as well as all standard modes of operation. The core of the multiprogramming, break-in and real-time operation problems has been identified with the indicator system of the Delta Computer.

Part I: General Description

Within the Delta Computer, the indicator register is proposed to be one word in length or 64 bits long. The register is categorically divided into five groups of control information and are positioned with the highest priority listed first and associated with the more significant bits of the register. The first or most significant group of indicator bits is tentatively named Machine Error Condition indicators and have as their main function, indicating specifically defined error conditions that the programmer, supervisory program, machine operator or maintenance personnel would be concerned with. Within this category might be indicator bits representing corrected error conditions (e. g. auto-correction code) which could be used as an indication that machine maintenance should be scheduled. (e. g. a pre-defined number of corrected error conditions within a prescribed time period could indicate maintenance is required in a specific area of the machine).

The second group of indicator bits are called Other Machine Assigning indicators and provide for computers or other machines external to the computer being considered to indicate to the computer being considered that external conditions are such that a break-in may be in order to control or take action because of these external conditions. Part III of this memo describes a possible mode of operation and indicator bit identification for this category of indicator bits.

The third group or Input-Output Conditions indicator bits encompasses all of the conditions that the programmer, supervisory program, etc. should possibly be concerned with relative to controlling input-output operations.

The fourth group of indicator bits named Internal Machine Conditions indicators reflects at this time the list of items due to actual machine operation that a program could possibly use to advantage in modifying its operations to compensate for recognizing decisions, faulty data, misprocessing, points reached, reminders, etc. Programming to handle special cases can be greatly simplified and speeded up by taking advantage of these indications and the break in facilities provided.

The fifth and final group of indicator bits are named the Program Identifiable Condition indicators and reflect past and present thinking concerning the alteration switch philosophy. Group five has two parts, one part controlled internally by a program only, the second part controlled externally by appropriate selector switches (or particular pieces of machinery). This gives the program the ability to remind the computer at some later time of certain conditions identified now, or the ability to modify present or future operations based upon external conditions.

Certain properties of the Indicator Register and indicator bits should be restated or defined to fully understand the system. The Indicator Register is addressable by a computer and may have its contents stored in memory, or may have its contents replaced by a word from memory. The bits within the register are set (turned on) by conditions stipulated in identifying the bit. Some bits have bi-polar properties and are marked with an asterisk(*) on the list. These marked bits have the property of being able to be turned off as well as on as a result of machine operations. Consider for example the compare result bits 45, 46, 47, 48 of group four. At the end of a compare instruction assuming the result was equal, bit 45 would be set and 46, 47, 48 would be reset (turned off). The bits would remain in this state until the end of the next compare operation when the new results would be specified by the indicator bits 45, 46, 47 and 48. If the new results indicated low, then bits 46 and 48 would be on and bits 45 and47 would be off.

All of the bits are subject to be turned on or off by specific instruction designation and only the unmarked bits (not bi-polar, no asterisk mark) will be turned off when interrogated by a program. The specific bit causing a break in will be reset, its identity is retained in the Left One Counter (See Delta Computer Instruction Control System or Delta Computer Memo No. 15).

Part II Listing of Indicator Bits

Group 1 Machine Error Condition Indicators

00 Data Transmission error, uncorrected
01 Data Transmission error, corrected
02 Arithmetic error
03 Illegal or Erroneous instruction
04 Control Equipment error
05 unassigned
06 unassigned
07 unassigned

Group 2 Other Machine Assigning Indicators

08 No specific name assigned to each of these indicators.
09 The priority for break-in is held for bit 8 with priority
10 diminishing toward bit 15. See explanation for identi-
11 fication and use of these bits.
12
13
14
15

Group 3 Input-Output Conditions Indicators

16 Instruction reject
17 Exchange busy
18 Interrogation Response
19 Instruction Response
20 I/O unit R/W error
21 I/O data transmission error
22 Exchange data error
23 Control circuit error
24 I/O unit End of File
25 I/O unit Not Ready
26 I/O unit busy
27 Operation Request twice
28 Operation Request once
29 unassigned
30 unassigned
31 unassigned

Group 4 Internal Machine Conditions Indicators

32	Overflow Fixed Point
33	Overflow Floating Point (exp)
34	Underflow Floating Point (exp)
35	Lost Significance Floating Point (mant. "0")
36	Divide by zero attempt
37	Improper divide
38	Index sense zero
39	Index sense equal
40	Indexed address overflow
41	Indexed address negative
42	Index quantity overflow
43	Zero result *
44	Minus result *
45	Comparison result equal *
46	Comparison result unequal *
47	Comparison result high *
48	Comparison result low *
49	Z bit logical result *
50	R. T. Clock Hour of day reached
51	R. T. Clock Lapsed time period
52	unassigned
53	unassigned

Group 5 Program Identifiable Condition Indicators

54	Set by program
55	"
56	"
57	"
58	External Switches
59	"
60	"
61	"
62	unassigned
63	unassigned

Part III Explanation of Indicator Bits

00 Data Transmission error, uncorrected, implies that somewhere in machine operation a data error resulting from transmission was detected. The definition could imply that the error was detected in a machine area where no automatic correction exists or is possible, or that the error is one beyond the scope of the auto corrective technique employed.

01 Data Transmission error, corrected, signifies that an error in data transmission had been detected and corrected. The significance of the error is secondary - the primary purpose of introducing an indicator bit with these qualifications is to present a new philosophy whereby means can be provided to determine when machine operations are such that maintenance is required. The frequency of occurrence of this condition over a stipulated time period (program, hour, day, processing cycle) can be used as an indication of the machine's potential reliability. The frequency count can be accomplished by program counting or by automatic counting whichever is deemed more beneficial.

02 Arithmetic Error - any error detected in the arithmetic system or control area will be indicated here. Further investigation may reveal the necessity for more than one bit if the difference between two or more defined errors can be used advantageously. Also to be defined are the conditions which could possibly cause the indicator(s) to be turned on.

03 Illegal or Erroneous Instruction - this indicator bit is set when an instruction is decoded which defies, or attempts to execute operations not permitted by machine definition. One example could be an instruction attempting unsigned floating point arithmetic. This situation could arise if a programmer were careless, as a result of machine malfunction, or as a result of an attempt to use data as an instruction. This indicator bit in conjunction with other indicator bits could reveal much concerning the origin of the error.

04 Control Equipment error - any error that can be defined and detected relative to instruction execution control or logical control can be indicated by this bit.

05 Indicator bits are unassigned. Progress toward com-
06 pletely defining the computer should reveal how to best
07 assign meaning to these bits either as extensions of already defined bits, as combinations of defined bits or as indications of conditions not presently listed or identified.

08 These eight indicator bits comprise Group 2 of the logical
09 indicator groupings and are named the "Other Machine
10 assigning Assigning Indicators". These bits would be used
11 to specify that some computer external to the considered
12 computer wanted to communicate with the considered com-
13 puter. No fully detailed system is presently available, but
14 a potential system is outlined here for comment and criti-
15 cism. Assuming a machine concept similar to that of the Stretch machine, we can conclude that both the Delta and Sigma machines are each equipped with similar, but not necessarily identical indicator registers. If in the Sigma machine, the 64 bits of the indicator register are divided into 8 logical groups of 8 bits each, then each of the 8 bits in a group can be independently or'd together and fed to one specific bit of the other machine assigning group in the subservient machine. Therefore, in the Delta indicator register are found 8 bits named "the other machine assigning indicators" each one of which indicates whether or not a condition had been identified in any of 8 associated bits of the Sigma indicator register. There is no specific name assigned to any of these bits in the Delta indicator register. They indicate more than anything the priority of break-in conditions detected in the Sigma machine.

16 The Instruction Reject bit of the Delta indicator register is set by the Exchange whenever the Exchange, for any reason, finds that it cannot execute an instruction it had accepted from the Delta Computer.

17 The Exchange Busy Indicator bit indicates to the Delta Computer that the Exchange could not accept an instruction from the Delta Computer.

18 The Interrogation Response Indicator bit is set by the Exchange when an interrogation instruction has passed all tests in the Exchange and has been executed.

19 The Instruction Response Indicator bit is set by the Exchange when an instruction from the Delta Computer has passed all tests and is being executed. Operation of an input-output unit in conjunction with the instruction is mandatory. It is not implied that the instruction has completed execution or that no error has been or will be made in the execution.

20 The I/O Unit Read Write Error Indicator bit in the Delta is turned on by the Exchange when the Exchange identifies an error while working with an I/O Unit and that error can be attributed to the I/O unit.

21 The I/O Data Transmission Error Indicator is turned on by the Exchange when an error is detected which can be classified as a data transmission error between the I/O Unit and the Exchange registers.

22 Exchange Data Error. This indicator is turned on in the Delta by the Exchange when an error is detected which cannot be attributed either to the I/O Unit or the transmission process.

23 The Control Circuit Error Indicator is turned on by the Exchange when the Exchange itself determines an inconsistency in its own operations.

24 The I/O Unit End of File Indicator information is communicated to the Exchange by the I/O Unit. The Exchange in turn sets the indicator bit in the Delta Computer.

25 The I/O Unit Not Ready Indicator bit in the Delta Computer is turned on by the Exchange when in attempting to execute an I/O instruction, the Exchange discovers that the specified I/O unit is not ready.

26 The I/O Unit Busy Indicator Bit in the Delta is turned on by the Exchange when in the process of attempting to execute an I/O instruction, the Exchange finds that the specified I/O Unit is pre-occupied.

27 The Operation Request Twice Indicator bit is a new inno-
28 vation and presented here for consideration, comment and criticism. The function of this indicator bit is such that it cannot be turned on unless the operation request once indicator bit has already been turned on.

This provides the Computer with the ability to learn that it should have taken prior action and must now go through extra manipulations to correct for operations not performed. The Operation Request Indicator bit is turned on in the Delta Computer when an I/O Unit requests assignment through the Exchange. If more than one I/O Unit requests service and the computer has not provided service for the first requesting unit, it would help the programmer to know that more than one unit has requested service.

29 These indicator bits are presently unassigned. Further
30 consideration of machine functions will probably indicate
31 how best use can be made of these indicator bits.

32 The Overflow Fixed Point Indicator bit is set whenever as a result of arithmetic operations on fixed-point words, an overflow condition is identified.

33 The Overflow Floating Point Indicator bit is set by the Computer whenever the exponent of a floating point word overflows during an arithmetic operation.

34 The Underflow Floating Point Indicator bit is set by the Computer whenever an underflow is identified in a floating point word exponent during arithmetic operation.

35 The Lost Significance Floating Point Indicator bit is set by the Computer whenever a zero mantissa is identified as a result of floating point arithmetic operations.

36 The Divide by Zero Indicator bit is set by the Computer whenever an attempt to divide by zero is detected.

37 The Improper Divide Indicator bit is set by the Computer whenever in attempting to perform a division operation, it can be ascertained that any of the rules for the divide operation have been violated.

38 The Index Sense Zero Indicator bit is set by the Computer when it can be ascertained that the indexing limit has been reached through counter expiration.

39 The Index Sense Equal Indicator bit is set by the machine when the indexing mode stipulated is one that calls for the index quantity to reach a pre-determined level. This level is a result of a comparison and not counter exhaustion.

40 The Indexed Address Overflow Indicator bit is set by the Computer when the address resulting from an index operation has caused or has resulted in an address overflow. This address overflow is relative to the amount of physical memory attached to the machine at that given installation.

41 The Indexed Address Negative Indicator bit is set by the machine when in the case of indexing by decrementing, the resultant address is negative.

42 The Index Quantity Overflow Indicator bit is set by the machine whenever the modification to the indexing quantity results in the quantity overflow.

43 The Zero Result Indicator bit is set by the machine whenever as a result of an arithmetic operation, a zero word is detected.

44 The Minus Result Indicator bit is set by the machine whenever a negative number is the result of an arithmetic operation.

45 The Comparison Result Equal Indicator Bit is set by the machine whenever an equal is determined as a result of a comparison.

46 The Comparison Result Unequal Indicator bit is set by the machine after a compare operation has resulted in either a high or low but not equal condition.

47 The Comparison Result High Indicator Bit is set by the machine whenever as a result of the comparison, the principle word involved is high.

48 Same as (47) except comparison result is low.

49 The Z Bit Logic Result Indicator bit is set by the machine whenever as a result of a logical operation, a positive indication is determined.

50 The Real-Time Clock Hour of the Day Reached Indicator bit is set when the real-time clock reaches the point where it had been set as an alarm.

51 The Real-Time Clock Lapsed Time Period Indicator bit is turned on whenever the lapsed time has been measured by the clock. The clock can be set to measure small time intervals and it is desirable to determine when this small time interval has expired.

52 These indicator bits are presently unassigned.
53

54 These indicator bits can be called internal program set al-
55 teration switches. They provide a means for the Computer
56 to remind itself at a later time of conditions presently known
57 to the Computer.

58 The External Switch Indicator bits are basically the same
59 as alteration switches of present day computers. They
60 provide a means of communicating to the computer via ex-
61 ternal switches. These external switches can in reality be machines, other computers, or actual switches.

62 Unassigned.
63