Suffrit
49.1

COMPANY CONFIDENTIAL

PROJECT STRETCH

FILE MEMO # 63

MEMORY BUS FILE MEMO #3

SUBJECT: Description of an Improved Bus System
BY : R. T. Blosk
J. W. Fairclough
DATE: July 26, 1957

MEMORY BUS SYSTEM

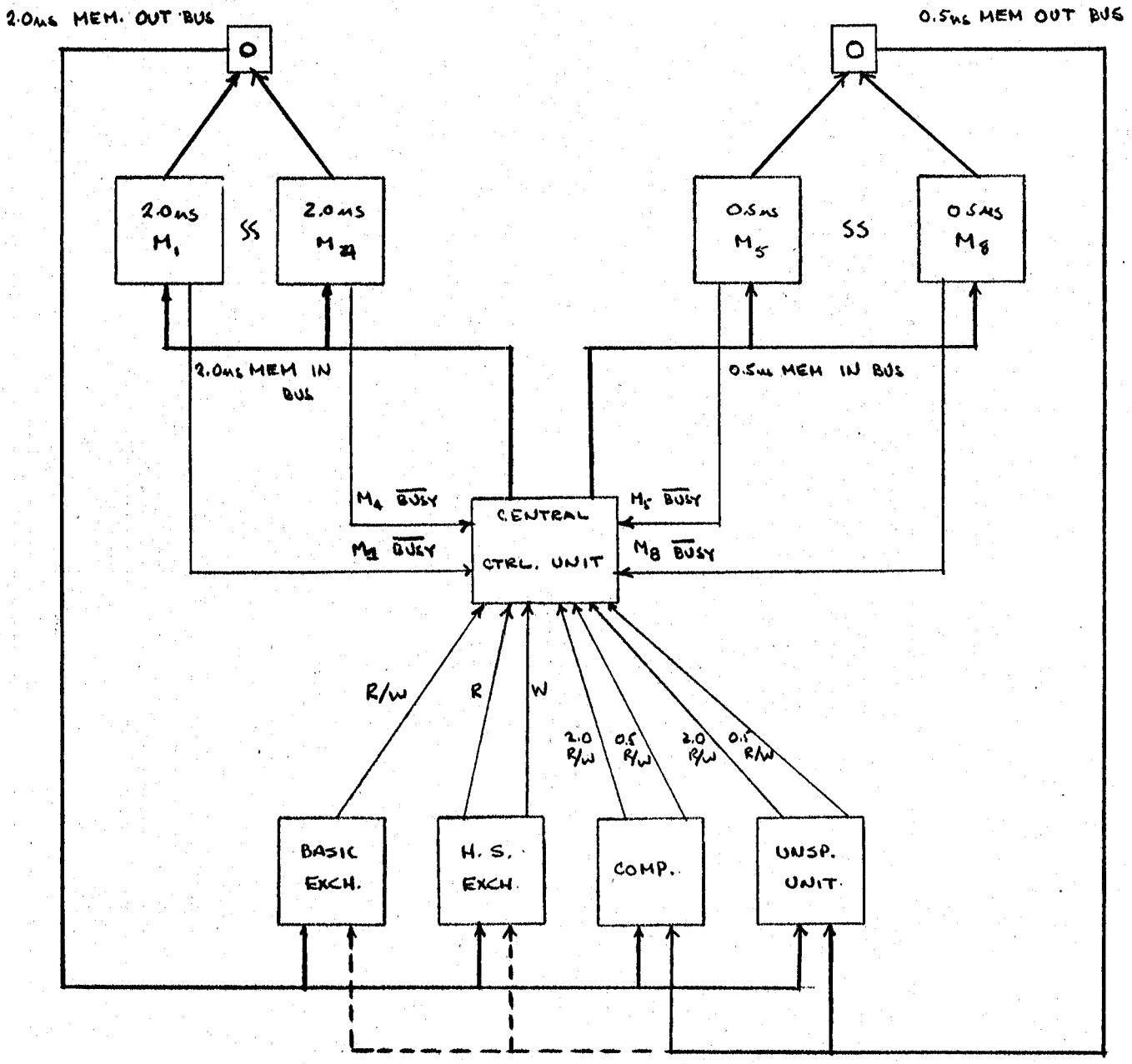

FIG. I

7/24/57
RTB
JWF

Project Stretch File Memo #63
Memory Bus File Memo #3

Description of an Improved Bus System

I. Introduction

The purpose of this memo is to describe a proposed memory bus system. The design is a development of the Clock Controlled Double bus system previously described in Stretch Memo #61 in conjunction with improvements derived from the many fine comments and suggestions received from other design and planning groups. It incorporates a number of new concepts which it is believed enhance the efficiency and usefulness of the bus.

II. Design Objectives

The design criteria of the bus remains the same as for the previous system where the bus must provide communication between a number of asynchronous computer units and a multiple set of asynchronous memories. It should provide sufficient capacity to ensure that the bus does not impose an operating limitation on the required data transfer rates of the various units in the system. In addition, the access times to the individual memories must be kept to a minimum.

III. General Description

Figure 1 shows the general arrangement. The 2 us and 0.5 us memories would each be provided with a memory IN and memory OUT bus.

The memory IN busses would each consist of the following lines:

- 14 Memory Word Address
- 1 Parity
- 64 Data Word
- 8 E. C. C.
- 1 Read/Write Control
- 7 Return Address
- 1 Parity
- M Memory Frame Select where M = number of memories

The memory OUT busses would each consist of the following lines:

- 7 Return Address

1 Parity
64 Data Word
8 E. C. C.
C Computer Select where C = number of computer plus exchanges

A central control unit provides the link between the computers and memories such that:

(1) A computer only communicates with a memory which is "not busy". An indication of the "busy", "not busy" condition of each of the memories would be maintained and compared with the memory frame selected before proceeding.

(2) The data would be switched to one of the two memory IN busses which would be determined by the memory frame selected.

(3) On each of the IN busses, priority would be established in the cases of simultaneous requests to memory frames on that bus.

This priority would be:

Basic Exchange,
High Speed Exchange,
Basic Computer, } ?
Harvest, or Sigma }

(4) Information would be positioned in discrete time intervals or slots, on each of the memory IN busses. The slots would be of equal duration and defined by a common clock.

(5) In the slot time during which information is put on a memory IN bus the "not busy" indication of the memory addressed would be changed to "busy".

(6) A memory frame decoder would be associated with each of the computer bus input paths so that:

a) A comparison with the "busy","not busy" condition of the memory designated could be made.

b) A memory frame select line could be energized in the same slot time as the information is put on the bus.

It may be found desirable for the computers to be able to make simultaneous requests to both 0.5 us and 2 us memories. This could be accomodated by providing two inputs from each of these computers, one for each bus. It is apparent however, that this necessitates control within each computer in order to determine which bus is selected.

It would be arranged that memories on the same bus, when requested, would start their cycles spaced by an integral number of slot periods from each other. This would occur naturally if the delay in travelling between the central control unit and the memories, plus the delay in starting the memory clocks were equal. Consequently it could be arranged that the memory clock provides a timing pulse to gate the information onto the common OUT bus which would never conflict with information from another memory frame. Therefore no control or priority arrangement would be necessary on a memory OUT bus.

A computer which communicates with both 0.5 us and 2 us memory must be able to receive data from the two memory out busses. However, in the case of Basic Exchange and High Speed Exchange the simultaneous return of information on both busses would not be possible because of their cyclic nature. This indicates that the input switching arrangement could be relatively simple. This is not the case, however, for a computer where the simultaneous return of information on the memory OUT busses must be accomodated. The manner by which this can be accomplished has yet to be worked out, however several methods are under consideration by the Bus and Computer design groups.

In order to approach 100% overlapped operation of a memory unit it is proposed that the memory should indicate "not busy" some time before the data is required in order to compensate for the control and transmission delay. If it is assumed that a slot is immediately available to a computer then this delay would be approximately 300 mus, and 100% overlapped operation could be achieved. However, a slot may not be immediately available, in which case the memory would be delayed in starting a cycle by as many slot periods as the computer had to wait. The worst case in this respect would be H. S. Exchange, Basic Exchange, Basic Computer and Harvest all simultaneously requesting memory frames, which are not busy, in which case Harvest would have to wait 3 slots before it could obtain a slot. The probability of this occuring appears slight and it is believed that in this respect 100% overlapped operation should be achieved most of the time.

An alternative method would be for the central control unit to contain memory cycle timers which would be initiated by a slot being sent to a memory and would later indicate when the memory was free again with no communication required from the memory unit.

IV. Basic Advantages of Proposed System

1. An IN bus is only used for communication with a "not busy" memory thus avoiding the need for acknowledgment and retransmission of the request if a memory is busy which was the arrangement under the system described in Memo #61.

2. Separate busses for the .5 us and 2 us memories ensure that:

   a) An accurate prediction of the access time to any Memory frame can be made and under no circumstances can .5 us memory block the return of information from 2 us memory which was possible on a common bus where .5 us memory was given priority. It was necessary for .5 us memory to have top priority on the OUT bus because of the limited time available to empty the OUT registers before the next cycle. Even when given top priority, there was a problem in accomodating an overiding priority for an Exchange read request from memory which was necessary to ensure fast access to Exchange units. This fact may have required the addition of extra registers in memory for buffering to the OUT bus.

   b) A 200 mus slot can be adopted and provide double the bus capacity, when compared with a single bus using a similar slot.

      A slot of less than 200 mus seemed possible on a single bus for both memories until the requirement of filling successive slots from one computer was considered which in the case of Harvest, at least, is desirable/essential. Also, a number of unknowns associated with the circuits, particularly with the complex switching and priority requirements of the single memory OUT bus configuration, made the proposal of a narrower slot difficult at the present time.

3. Due to the cyclic nature of both High Speed and Basic Exchanges it is necessary for the worst case access time to memory to be within certain limits which are a function of the cycle times. It has been determined that the system proposed satisfies these limits and satisfactory operation of both Exchange units could be achieved. The system described in Memo #61 would not fulfil these requirements.

V. Memory Access Time:

In order for the Basic Exchange to guarantee simultaneous operation of its I/0 units it must have access to words in memory within 4.5 us. The worst case access time for the Basic Exchange to 2.0 us Memory on the proposed bus system is as follows:

Basic Exchange (B. E.) to Central Control Unit (C. C. U.)	.100 us.
Selected memory just taken by other unit	2.000 us.
Just miss a slot on IN bus	.200 us.
Fill a slot on IN bus	.200 us.
Transmit time (cable and logical delay)	.100 us.
Mem. address decode time	.300 us.
Memory cycle read time	1.000 us.
Fill a slot on OUT bus	.200 us.
Transmit time	.100 us.
Total -	4.200 us.

This satisfies the Basic exchange requirements.

The average access time for any unit to obtain a word from 2.0 us Memory assuming the selected Memory is not busy is as follows:

Reg. to C. C. U.	.100 us.
On the average miss 1/2 slot	.100 us.
Fill a slot on IN bus	.200 us.
Transmit time (cable and logical delay)	.100 us.
Address decode	.300 us.
Memory Read time	1.000 us.
Fill Out slot	.200 us.
Transmit time	.100 us.
Total -	2.10 us.

For the High Speed (H. S.) Exchange to be satisfied, the worst case has to be considered where the Basic Exchange and both the H. S. Read and H. S. Write call for service simultaneously to the same memory. Also, another unit such as Harvest may just have gained access to that memory.

The timing that results is as follows:

Exchange to C. C. U.	.100 us.
Harvest takes the memory	2.000 us.
Basic Exchange gets it next and also misses a slot	2.000 us.
	.200 us.
H. S. Read just misses a slot	.200 us.
H. S. Read fills a slot	.200 us.
Total time	4.70 us.

This means that if H. S. Read is given priority over H. S. Write it can be serviced within 4.7 us. which is within its maximum rate of 1 word every 5.6 us.

H. S. Write may have to wait while a further Exchange cycle is satisfied but it would be assured of the one following and the data would be returned in approximately 10.5 us. This is greater than its maximum word rate of 1 word every 7.1 us. In order to guarantee successful continuous operation a second Write Register could be added which would allow an interval of 14.2 us before requiring the requested data word. Another method would be to use a look ahead feature where Harvest and all lower priority units are blocked from service to an individual memory under these worst conditions. This latter method has some apparent problems associated with it such as:

a) Accurately pre-determining the worst case condition when the Writing and Reading are both operating asynchronously with a constant Write cycle and a variable Read cycle.

b) Preventing the blocking of Harvest/Basic computers erroneously.

Both methods are under consideration by the Exchange design group.

VI. Checking

One check on memory addressing is accomplished by sending a parity bit to memory along with the 14 bit word address. During address decode time in the memory cycle a parity check is made on the address register and any error found is indicated.

A further check is made during the memory cycle by comparing the actual X and Y drivers selected against the address register and again an error encountered is indicated.

The Return Address received with data coming out of memory is parity checked when it is gated off the Memory OUT bus and accepted into the receiving unit. A single parity bit is transmitted along with the Return Address both to and from Memory.

All data word checking and correcting is assumed to be accomplished within the computer units before being placed on the Memory IN bus and after being taken off the Memory OUT bus.

VII. Summary

This memory bus system provides a much improved and more practical solution to the communication problems of the Stretch system.

1. It satisfies the anticipated maximum requirements of the Harvest computer as well as the Basic and High Speed exchanges.

2. The system is much more efficient because:

   a) The IN bus only transmits references to memories which are "not busy".

   b) The priority established on the IN bus is carried through the memories onto the OUT bus.

   c) Access times can be accurately calculated since the return of data from memories is not affected by varying priority situations on the OUT bus.

3. It provides greater flexibility in basic system arrangement and expansion by limiting the connection to the 0.5 us memory busses to only those units that require access to 0.5 memories. In addition it provides greater facility for increasing the number of memory units on the system.

4. The specified bus timings are not predicated upon the best circuit conditions and delays, and presupposes that future tests and special circuit designs may provide faster timings.

5. The address checking provided is relatively straightforward and simple with no waiting for an acknowledgment return. The data word checking and correcting would be done within the computer units.

6. By increasing the bus capacity the memories can more closely approach fully overlapped operation.

7. Each slot of information contains an energized Select line which conditions the gate of the addressed receiver and transfers the data off the bus in a minimum of time. No slot time is spent in decoding a binary address at the receiver.

This system has to be studied further in order to determine the limitation on the number of memories/computers which can be efficiently serviced. In addition, the complete range, from a small basic system, to a large powerful system has to be defined. It is felt that the proposed system may have sufficient flexibility to cover this range.

R. T. Blosk

J. W. Fairclough

RTB:JWF:bjn