COMPANY CONFIDENTIAL

PROJECT STRETCH

FILE MEMO NO. 52

SUBJECT: Clearing of Memory

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DATE: October 29, 1956

In statistical applications of the Stretch Machine memory locations are to be used as counters. It will be necessary to clear simultaneously any block of memory locations which are used for the counting operation. This memo will outline the possible methods of accomplishing the clearing, and some of the problems that will be encountered. The particular method to be used cannot be specified at this time, since the memory components are in the development stage. Selection of the method will depend upon the characteristics of the components.

The size of the area to be cleared will be on the order of 4 x 8 words in each of several memories or some multiple of this size. The block of memory used is distributed in several memories to allow for counting faster than the normal memory operation. It will thus be necessary to simultaneously clear a part of each of the several memories which are interleaved as a single operating unit for counting purposes. Distributing the block in several memories also reduces the technical problems, since the number of cores to be switched by each driver is reduced.

It is important that the clearing operation be accomplished rapidly, but not necessarily within a single memory cycle. Clearing within two memory cycles would be satisfactory; that is, within one microsecond for the fast memory and four microseconds for the large memory.

## Large Memory

There are several possible methods of clearing a block of locations in the two microsecond 64 x 128 memories. The most obvious method involves turning on all X and Y read drivers whose lines intersect within the block. Coincidence would be established in all cores within the block, switching them to the zero state. This assumes the use of a driver for each line, not a matrix switch.

Normally, the distribution of ones stored in a plane will be reasonably random, and the population of ones will be small. If so, during the clear operation, the cancelling property of the sense winding will limit the noise signal applied to the sense amplifier. The largest noise signal would be generated by a checkerboard pattern, in which alternate cores in each direction contain ones and zeroes. In this case, there would be no cancellation of signals. If the block to be cleared is 4 x 8, the signal out would be 16 times normal. Although the possibility of storing a perfect or near perfect checkerboard is very remote, limiting circuits should be included in the sense amplifiers to protect them from the noise impulses. Otherwise, the speed of the clear memory operation would be controlled by the recovery time of the sense amplifiers. Protection from any errors due to blocking of the amplifiers will be given also by the auto-correction mechanism, which is assumed will be a part of the memory system.

In a normal memory operation, only 64 cores can be fully switched simultaneously by one X or Y driver. In clearing a 4 x 8 block, however, it is possible that 8 x 64, or 512 cores could be switched. Increasing the number of switched cores increases the inductance of the system, reducing the speed of the switching process. This reduction is not in direct proportion to the number of switched cores, since the large number of half selected cores on the line also controls the inductance. For a clearing operation, therefore, it will be necessary to energize the drivers for a longer time than in normal operation. The slower switching speed in clearing has the advantage of reducing the signals induced in the sense winding.

Another possible method for clearing memory would use the inhibit windings. A separate inhibit winding would pass through all cores to be cleared. During a clearing operation, twice the normal inhibit current would be passed through the winding. The inhibit drivers would necessarily be capable of operating in two modes, a normal and clearing mode. This added circuit complexity makes the inhibit method look less attractive than that of using the X and Y drivers. However, if matrix switch drivers, rather than individual drivers, are used, the inhibit method could be used to advantage. The large number of switched cores would have the same effects as discussed before; that is, a slowing down of the switching, thus reducing the noise per core induced in the sense winding.

An extra winding could be provided for the sole purpose of clearing. This method would be unattractive because of the difficulty of threading another winding through the cores. This, however, would depend upon the size of core chosen. It has the advantage of using a special driver, which could have a slow rise and fall to prevent large noise signals from being induced in the sense winding.

## High Speed Memory

The high speed memories could also be cleared by turning on the necessary X and Y drivers. Most of the previous discussion still holds, with one exception. In the forms of high speed memory now being considered, the storage state of the cores has a relatively small effect on the inductance of the system. This is because magnetic flux in the cores is not reversed during a memory operation, but is switched between two paths. However, if a 4 x 8 block is to be cleared, twelve of the drivers will be loaded by the full selections of at least one fourth of the cores associated with the drivers. The line inductance would thus increase in greater proportion than in the large memory case. The drivers must remain on for several times the normal duration. This would still be fast, since the normal driver duration is expected to be only 0.1 microsecond.

Some of the forms of high speed memory under consideration require the use of a bias winding. If the bias winding is provided with switching circuitry which will turn off the bias current, it would be possible to clear these memories after removal of the bias. In some cases, the inhibit winding for the block should be energized with the normal value of current. In others, all the X drivers or all the Y drivers in the block should be energized. These methods have no apparent advantages over using the X and Y drivers, but are included for completeness. They require bias control circuits, while with other methods the bias windings are simply returned to a D. C. Supply.

An extra winding could be used for clearing, but is not advised because of the already complicated nature of the windings for normal operation. If a matrix switch type of driver is used, this will be necessary, however.

## Summary and Conclusions

Several methods for simultaneous clearing of memory have been discussed. The method to be used cannot be specified until the memory components have been developed.

The main considerations are the timing changes necessitated by increased inductance, and noise effects on the sense amplifiers.

Discussions in this memo have been qualitative because of the status of memory development. As the memory development proceeds, data will be available and the clearing problem can be examined in more detail.

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