J. E. Griffith

COMPANY CONFIDENTIAL

PROJECT STRETCH

FILE MEMO #49

SUBJECT: Timing Diagrams
BY: Mr. J. E. Griffith
DATE: October 17, 1956

This memo sets forth a trivial example of timing, using assumptions that are stated on the sheets. The purpose of this memo is to illustrate the basic method of generating a timing diagram which will be a function of all of the following:

1) an assumed machine organization
2) an assumed program
3) an assumed assignment for data in the memories

The timing diagram will display, in time, the machinations necessary to perform the work specified by the program, and when finished, it will allow one to measure the coupling constants between the three sets of assumptions stated above.

It is suggested, as a general rule, that timing diagrams be drawn on paper from which Ozalid reproductions can be made (preferably paper which will reproduce the grid lines).

Roger's Inner Loop: October 1, 1956 - J. E. Griffith

Notes on Timing Diagram

μsec 0.5 - Constants such as Jm should probably be stored in IM.

1.9 - FM reference for Instruction 2 is delayed in accordance with Rule 1.

2.1 - MM reference for α is stored at 2.1. Instruction 1 is assumed to drop instantaneously into decoder from which MM_1 is fired.

2.9 - FM reference for Instruction 3 is delayed by Rule 1.

3.1 - Instruction 2 drops into execution controls, but cannot actually start execution until μsec 3.7.

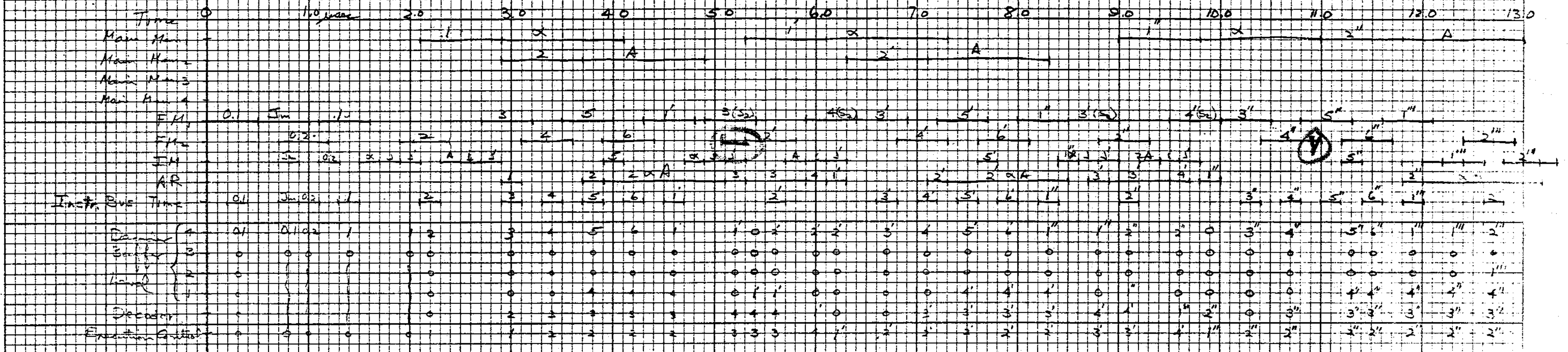
3.9 - Instruction 5 is executed in level 4, thus it no longer exists at μsec 4.1.

4.2 - Instruction 6 is also executed in level 4, Note that FM reference for next instruction does not start until bus has settled down at μsec 4.3. Same is true at μsec 3.1 and 4.5.

5.9 - FM RI started with the actual "store" operation.

6.1 - FM reference for 3' would start at this time except for FM conflict.

Rogers Inner Loop 10/1/56 J. Griffith



FM Program assignment

1 0.1 $J_m \rightarrow J'$

2 0.2 $0 \rightarrow S_2$

1 1.0 R Add α

Sub J

Sub J'

2 2.0 Mpy A

Sub i

Sub j

1 3.0 Add S_2

2 4.0 Store S_2

1 5.0 J'-1 E Test

2 6.0 Tr to 1.0 if J'-1 not zero

Data Mem Assignments

Cycle	1	2	3
Data			
α	MM_1	MM_1	MM_1
A	MM_2	MM_2	MM_1
S_2	FM_1	FM_1	FM_1

Rules

1) Start FM reference for next instruction at beginning of last indexing operation on present instr. (e.g. [illegible] =)

2) Main Mem RO can be initiated only from Decoder B. Level #2 or below for Arith instructions

3) Main Mem RI can be initiated only from Execution controls for Arith instructions

4) FM RO will be started 0.2 μsec before end of present Arith execution (e.g: μsec 4.9, 8.5)

5) FM RI same as Rule 3 for MM (e.g: μsec 5.9, 9.5)

6) All address modification occurs in level 4

7) Instructions remain in Execution Controls until execution is finished. (e.g. Instr #1.0, 2.0, 1.0, 2.0 etc.

8) assume a separate FM-to-Decoder Bus and a Main Mem-to-AR & Decoder Bus.

Comments

1. The first two cycles are carried out to show general principles; cycle #3 shows a MM conflict.

2. Rule #1 prevents "α-Store Add α+1" type of conflict

3. Instructions will generally be decoded in the decoder while awaiting "end of operation" signal from prev. instr.