October 29, 1956

Memorandum to: Mr. S. W. Dunwell

From: Stretch Product Planning Group

Subject: Addressing Scheme for the LINK-LASL Computers

As presently proposed the Stretch System consists of the LINK and the LASL computers. It has also been proposed that the memories mutually available to the two computers provide memory access speeds of 0.2, 0.5, and 2.0 microseconds. It has been agreed that the words within these memories be specified by addresses given in a binary integer notation. In considering various machine operations and the methods to be used in controlling the LINK-LASL computers, the assignment of addresses is of importance. The purpose of this memorandum is to present a proposed scheme of addressing. This scheme was devised to:

1. Present a minimum of logical inconvenience to the programmer.

2. Provide LINK with nominally independent memory facilities.

3. Maintain a consistent addressing scheme compatible with increased memory capacity.

MEMORY ARRANGEMENT

Figure 1 serves to illustrate the way in which the memories are related and used in the two machines. As presently conceived, one central bus connects the I/O Exchange, the Link Computer, and the LASL Computer with the various memories. Connections to some of the memories with the central bus are made under certain particular conditions. These conditions are under the control of the programmer, or become effective provided automatic machine correction has been specified. In normal operations the faster memories operate over a separate bus to the associated arithmetic and control registers of a particular computer.

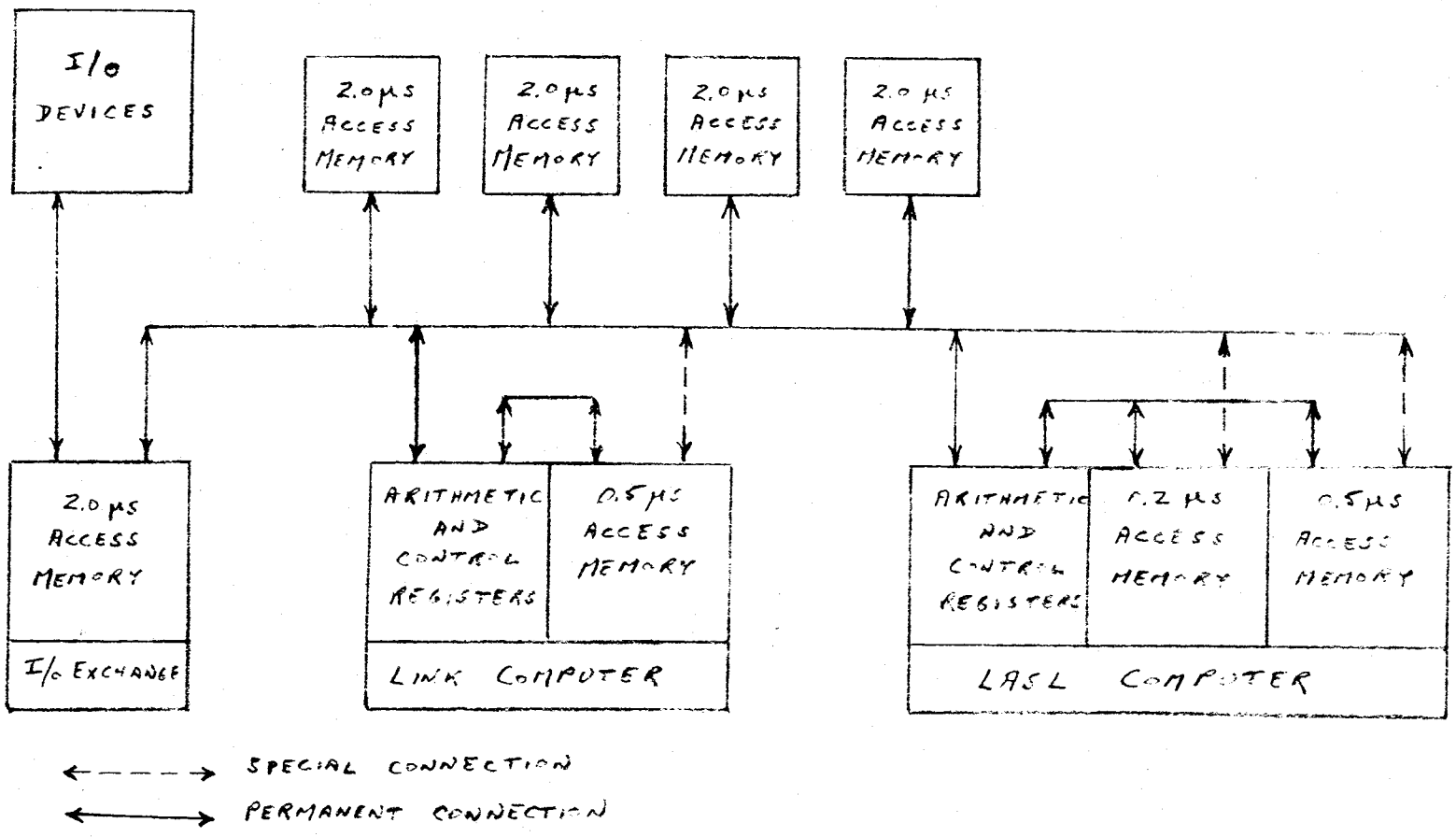

FIGURE 1. MEMORY ARRANGEMENT FOR LINK-LASL SYSTEM

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The 2.0 microsecond access memory is available to all three component machines. The degree to which the three machines may compete for the use of the central bus is being investigated. It is expected that a central bus may be able to handle the traffic anticipated. It is likely, however, that competition for the 2.0 microsecond memory boxes may result in excessive delays in the LASL Computer. If this is true, then the LINK machine may require a separate 2.0 microsecond memory for operations of its own plus those connected with the I/O Exchange.

PROPOSED SCHEME

The following scheme of addressing, using the specified memory for the LASL computer and some additional memory for the LINK Computer, is proposed:

Decimal Address	Octal Address	LASL Meaning	LINK Meaning
0	0000000	No Address	No Address
1 to (3,055 -x-y)	0000001 to (0005757 -x-y)	Storage Selection Error	Storage Selection Error
(3,056 -x-y) to (3,055 -y)	(0005760) to (0005757 -y)	Storage Selection Error	LINK Internal Registers (x)
3,056 -y) to (3,055	(0005760) to 0005757	LASL Internal Registers (y)	Storage Selection Error
3,056 to 3,071	0005760 to 00057770	0.2 microsecond Memory (LASL)	Storage Selection Error
3,072 to 3,583	0006000 to 00067770	0.5 microsecond Memory (LASL)	Storage Selection Error
3,584 to 4,095	0007000 to 0007777	0.5 microsecond Memory (LASL)	0.5 microsecond Memory (LINK)
4,096 to 32,767	0010000 to 0077777	2.0 microsecond Memory (MAIN)	2.0 microsecond Memory (MAIN)
32,768 to 2,097,151	0100000 to 7777777	Storage Selection Error	Storage Selection Error

DETAILED COMMENTS

The following explanatory comments will serve to describe the addresssing scheme. Certain assumptions concerning the uses of memory in the LASL and the LINK machine are also made. The cut-off point in memory addressing was set at 4,096. Further investigation may indicate that 2,048 is a better starting point for the 2.0 microsecond memory.

1. No address in the case of address $(0000000)_8$ implies that the indicated operation will be performed without a reference to memory. Thus, the number or data already in the registers will be used in the arithmetic operation specified.

2. A storage selection error will be defined by the programmer as a result of the action specified following the break-in function. It should be noted that the memory addresses have been specified so that one may index from one type of memory to the next without incurring a storage selection error.

3. It must be possible to address specifically all of the internal arithmetic and control registers of the LASL computer and also all of the internal registers of the LINK computer. This is essential for status interrogation of each of the machines. It also provides additional flexibility in the normal operation of a given machine.

4. Any word of selectors which are directly associated with the LASL machine may be referred to by one of the addresses specified in the set of internal register addresses. A similar statement is applicable to selector registers associated with the LINK machine. Those selectors referring to input-output status or control are associated with the I/O Exchange unit. As such, this information is available to either the LINK or LASL machine at any time. The addresses of such selector registers is assigned in the input-output class of instructions. For this reason, these addresses are independent of the addressing scheme being defined.

5. The internal register addresses are given specific addresses above. It is preferable that the LASL addresses be in sequence with the 0.2 microsecond memory, so that block transfers may be specified through appropriate indexing.

6. It is presumed that the 0.2 microsecond transistor memory will be allocated in the usual case to the LASL computer. It is not useful in the LINK machine.

7. It is presumed that the 1000-plus words of 0.5 microsecond memory will be allocated in the usual case to the LASL computer, but some 0.5 microsecond memory will be required by the LINK computer. The 0.5 microsecond in LINK is analogous to the 0.2 microsecond memory in the LASL computer. Indexing and the temporary storage of results require that some meory of this type be provided for the exclusive use of LINK. This addressing scheme assumes that LINK will always have some 0.5 microsecond memory. If this were not true, indexing would be impossible since tag addresses do not extend to the 2.0 microsecond memory.

8. The MAIN memory of 2.0 microsecond access memory is accessible equally to either of the machines.

9. There will be some cases where it might be necessary for LINK to obtain information from a fast memory associated with the LASL machine, or from one of the internal registers of the LASL machine. Similarly, cases will arise where it will be necessary for the LASL machine to obtain information from a fast memory associated with the LINK machine, or from one of the internal registers of the LINK machine. It is felt that situations of this type will be exceptional cases, and, thus may be defined by an appropriate bit in an instruction or a special instruction specified by the machine requesting the information. These special requests for information within the other machine will always imply that the machine containing the information will always reach a suitable stopping place before the information request is granted. For example, if the LINK requests information contained in the fast memory of the LASL machine, both the control decoder and the execution control of LASL must complete assigned actions before the request can be granted. In the normal case, in which such operations will be used, it is anticipated that one of the two machines will have obtained control of the system. Thus, the machine, upon which requests for information are being made, is operating as a "slave" to the machine making the request.

10. It will be necessary to specify a "lock-out" address within the 2.0 microsecond access memory. This "lock-out" address operates upon the high order nine bits only. By an appropriate setting one may cause the LASL computer to use its normal address structure up to the lock-out address. The LINK machine is permitted to use all of the addresses up to $(0007777)_8$ in the normal manner. The LINK system may also use the 2.0 microsecond memory from the lock-out address to the highest address of memory. This should simplify the operation of the LASL and the LINK machines as separate systems. As an example, if the lock-out address is specified as $(002)_8$, then the 2.0 microsecond memory in the previous example has been apportioned as:

LASL	$(00100000)_8$ to $(0011111)_8$
LINK	$(0020000)_8$ to $(0077777)_8$

In this case, the block of addresses assigned to the LASL Computer are not available to LINK, and similarly, the higher block of addresses assigned to the LINK machine are not available to the LASL Computer. Addresses within this structure can be made available only through the same mechanism described in the previous section.

11. With respect to the 2.0 microsecond memory, it is probably well to state at this point that the LASL Computer will have requirements for the 28,000 plus words of memory provided. The LINK will also require a memory of its own. The sequencing in addressing through the four blocks of 2.0 microsecond memory in the LASL Computer is essential. It is presumed that a similar amount will not be available to LINK. With the "lock-out" described in the preceding section a combination of time-sequenced and non-time-sequenced memory can be made available to LINK.

12. It has been assumed that each block of 0.5 microsecond memory will consist of 512 words, an address register, and a memory register. Each block of 2.0 microsecond memory will consist of 8,192 words, an address register, and a memory register. In the recommended address structure, it should be noted that all of the special addresses and the higher-access speed memories replace 4,096 words of 2.0 microsecond memory.

INCREASED MEMORY CAPACITY

If a customer would like to order additional memory, for example, an additional 16 transistor register, an additional block of 512 words of 0.5 microsecond memory, and two blocks of 8,192 words of 2.0 microsecond memory, the address structure for the LASL and the LINK machines is as follows:

Decimal Address	Octal Address	LASL Meaning	LINK Meaning
0	0000000	No Address	No Address
1 to (2,543 -x-y)	0000001 to (0004757 -x-y)	Storage Selection Error	Storage Selection Error
(2,544 -x-y) to (2,543 -y)	(0004760 -x-y) to (0004757 -y)	Storage Selection Error	LINK Internal Registers (x)
(2,544 -y) to (2,543)	(0004760 -y) to (0004757)	LASL Internal Registers (x)	Storage Selection Error
2,544 to 2,559	0004760 to 0004777	0.2 microsecond Memory (LASL)	Storage Selection Error
2,560 to 3,071	0005000 to 0005777	0.5 microsecond Memory (LASL)	Storage Selection Error

Decimal Address	Octal Address	LASL Meaning	LINK Meaning
3,072 to 3,583	0006000 to 0006777	0.5 microsecond Memory (LASL)	Storage Selection Error
3,584 to 4,095	0007000 to 0007777	0.5 microsecond Memory (LASL)	0.5 microsecond Memory (LINK)
4,096 to 49,151	0010000 to 0137777	2.0 microsecond Memory (MAIN)	2.0 microsecond Memory (MAIN)
49,152 to 2,097,151	0140000 to 7777777	Storage Selection Error	Storage Selection Error

In this case the block of memory from 4,096 to 32,767 (decimal) is sequenced through four blocks of memory. Thus, the location of a few words is indicated as:

Memory	Addresses
Box 1	4,096 - 4,190 - 4,104, etc.
Box 2	4,097 - 4,101 - 4,105, etc.
Box 3	4,098 - 4,102 - 4,106, etc.
Box 4	4,099 - 4,103 - 4,107, etc.

The block of memory from 32,768 to 49,151 is apportioned as follows:

Box 5	Addresses 32,768 through 40,959
Box 6	Addresses 40,960 through 49,151

The programmer can obtain higher-efficiency of operation by optimumly programming the use of addresses in boxes 5 and 6. The address structure automatically optimizes references to boxes 1 through 4, in most cases.

This arrangement emphasizes the importance of assuming that additional memory will be obtained in terms of four boxes of 8,192 words.

LINK AS INDEPENDENT SYSTEM

The assignment of addresses as described above can be used on an independent LINK machine without too much inconvenience. It has been assumed that the LINK machine will always have some 0.5 microsecond memory available to it. It may be necessary to consider that 2.0 microsecond memory starts at 2,048 or even 1,024 in an independently operated LINK machine. The suggested addressing scheme is satisfactory for present purposes. Consideration should be given to an improved system for independent LINK machines.

INPUT-OUTPUT EXCHANGE

The address structure as relating to the Input-Output Exchange is independent of the above assignments, since any reference to the memory of the exchange will be considered as an input-out class instruction. Thus, rather than to RESET and ADD information coming from the exchange control registers, one will QUERY the status of such registers. This permits an independent selection system. In fact, these addresses may correspond to the block of storage selection error indications immediately following a zero address and just ahead of the block of addresses assigned to the LASL Internal Registers. It is considered essential that either of the two machines, LASL or LINK, be permitted to query the status or condition of any of the exchange registers.

CONCLUSION

An addressing scheme for a LINK-LASL system was presented in this memorandum. Certain assumptions were made concerning the provision of a separate 0.5 microsecond access memory for LINK. A means for isolating or locking-out a portion of the 2.0 microsecond for LINK and from the LASL computer was proposed. The system was generalized by providing a means by which either machine could use the memory assigned to the other machine. This mode of operation is under control of the programmer. The method by which the addressing scheme would be extended to increased memory capacity was shown. It was indicated that the addressing scheme was satisfactory during independent operation of the LINK machine. A brief comment on the Input-Output Exchange addresses was made, and these addresses were shown to be independent of the major system.

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