COMPANY CONFIDENTIAL

THE LINK EXCHANGE

H. K. Wild June 13, 1956

Introduction

The Input-Output Communication System will provide the means to transfer information between the main memories of the STRETCH Machine and the peripheral and terminal equipment which will be used in conjunction with the computer. The communication System is called the LINK Exchange because of its similarity to a telephone exchange.

By command of the LINK Computer, the Exchange will establish and maintain information channels and otherwise control the input-output units. These units will consist of High Performance Tapes and RAM, and low speed devices such as 727 tapes, Card Readers, Document Readers, Printers and Punches and Direct Action devices such as keyboards and telemetering equipment.

Generally speaking, the LINK Exchange will provide buffering in memory. It will have the ability to handle a large number of input-output units simultaneously, regardless of speed, up to and beyond present tape speeds. The Exchange unit will contain all multiplexing controls which in itself leads to employing new devices and techniques.

A considerable amount of investigation has been made in the area of low speed devices. This report will generally be limited to this area. Modifications of the methods described will be necessary to extend the system to the area of high speed tapes and high performance RAM.

It is anticipated that the memories serving the LINK System will have a memory cycle of 2 usecs and that the word size of the memory will be in the order of 60 bits.

Figure I illustrates the relationship of the LINK Exchange to the LINK system.

The LINK Exchange will perform the following functions:

1. From the input devices, it will accumulate 6-bit characters into 60 bit words and store these words at the desired locations in the main memory.

2. It will transfer information from designated locations in the main memory to output units. Since many of the output units will not accommodate words of 60 bits, word sections will be formed of the required size for transfer to these output units.

3. It will provide for simultaneous operation of several input and output units and many direct action devices while the LINK System is computing. The ability for an input or output unit to be connected into any channel currently not in use will be provided.

4. After receiving the initial command from the LINK Computer to execute reading, writing or control functions with a given I/O unit, the LINK Exchange will execute the required instruction independently of the computer, so that the computer can do other things during input-output operations.

Operation (See Figure 2)

It is assumed that except for High Speed Tapes and High Performance RAM, this data will be transferred between the I/O units and the accumulating memory six bits at a time.

A command to Read from or Write to a specified unit will be given by the LINK Computer. The conditions necessary for the execution of the instruction, i.e., the Ready status of the unit addressed and the load on the LINK Exchange would first be sampled.

The LINK Exchange will assign an information channel to the unit through the magnetic core crosspoint switch. The control word will be entered into the accumulating memory at the address associated with that channel. After setting up the channel and storing the control word, the unit is started and the LINK Exchange is ready to make another assignment.

Information arriving from a unit is temporarily stored at the associated intersection in the magnetic core crosspoint switch. The columns of the switch are sequentially sampled and the data stored there is transferred to the associated data word location in the accumulating memory.

As each six bit section is entered into the accumulating memory, the respective data word is shifted six places to the left. The process continues until 60 bits from a particular unit have accumulated. This is signified by a count which is kept with the data word. When the data word has been completed, it is written into the main memory at the address specified by the control word.

When writing, the information is taken six bits at a time from the accumulating memory and stored in the appropriate intersection in the crosspoint switch, until called for by the output unit.

During each data word memory cycle, the word is shifted to the left six places to bring the next six bits into position for the following memory cycle. A subcycle count is kept with the data word. When ten subcycles have been taken, the LINK Exchange obtains the next word from the main memory at the address specified by the control word.

Data can be transferred between the main memory and several selected input or output units operating in an asynchronous fashion simultaneously by setting up several information paths through the magnetic Core Crosspoint switch.

Orgainization

To provide the facilities just described, the LINK Exchange will contain these significant features:

1. Multiplexing network. A magnetic core crosspoint switch, will allow several information channels to be set up between LINK and its peripheral equipment. A second level switching array will allow connection to a large number of direct action devices.

2. Accumulating memory. This will be a 2 usec. core memory of sufficient capacity to allow temporary storage of a 60 bit data word for each input and output device required to operate simultaneously. Between this memory and the low speed input-output units, data will be transferred in six bit sections of the 60 bit word. Therefore, directly associated with the accumulating memory will be circuitry to allow shifting the data word six places to the left each time it is read out and written back in.

   The accumulating memory is shown in Figure II as being a separate memory for purposes of clarity. However, a small portion of the main memory of the LINK System, with some modifications, can be set aside for exclusive use by the LINK Exchange. The main memory would then be time shared between input-output units operating at 727 tape speeds, approximately 80% of the time is available for computing. In the much larger systems that are contemplated, where an exchange may be required to handle the input-output data flow for more than one LINK, a separate small accumulating memory can be provided.

   Whether the accumulating memory is a portion of the main memory or is a special small memory depends upon the application.

3. Control Word. When an input-output unit is selected and the command given to Read or Write, a control word is stored in the accumulating memory in an address associated with the selected unit. The control word contains a memory address and a word count. The memory address designates the address in the main memory where the first word is to be read from or written to. As each successive word is transferred, the memory address is stepped up by one. The word count designates the number of words to be transferred. As each successive word is transferred, the word count steps down by one.

4. Control Word Modification. Each time a data word is transferred, the control word must be modified so as to step up the current memory address and to step down the word count. It is desirable that the control word be read out of the accumulating memory and written back modified during the same memory cycle. The device illustrated in Figure 3 will accomplish this. It consists of a simplified parallel adder with only one set of inputs and the carry circuits. The output of the device is the input binary number advanced by one (in the case of stepping up).

   For each order of the binary number one Exclusive OR logical connective and an AND connective are needed.

   Minimizing the carry time is accomplished by avoiding carry propagation. Each successive higher order of the binary number will AND all the preceding lower order inputs limited by the number of inputs possible to one AND circuit. A carry is then propagated and the process is repeated. Therefore, instead of requiring a carry propagation time for each order one every five or six orders would be possible, reducing the carry time to a large extent.

   There is evidence to show that a new component that will perform the exclusive OR functions may be realized. This is only one of the many applications where such a device would prove extremely useful and development of this component will be emphasized.

   For stepping down by one, an expression may be derived in a similar manner which has the logical form -

$$n_o = \bar{n}_i + \left[(n-1)_i \vee (n-2)_i \vee \ldots \ldots \ldots \ldots \vee 2_i \vee 1_i\right]$$

   where n represents a given order of the binary number.

5. Priority access to the main memory. Although data transfer and computing can be carried on concurrently, priority must be given to the input or output communications. Therefore, when a complete data word has been formed on reading or a new data word is needed when writing, this requirement takes precedence over computing. Interlocks will be provided to prevent a memory reference for computing when the LINK Exchange calls for a memory cycle.

Magnetic Core Crosspoint Switch

Of prime consideration in the design of the STRETCH Computer is reliability. Early in the investigations pertaining to the LINK Exchange, it became evident that for the approach considered, a form of crosspoint switch was necessary. It was felt that the familiar form of mechanical crossbar switch would not fulfull the requirement of extreme reliability.

A proposal was made to Dr. M. Haynes and Mr. L. Russell that core devices be investigated for this purpose. This investigation resulted in the development of a multiple hole structure with some unique properties. Figure 4 illustrates the manner in which the device would be used in a crossbar switch.

To select a particular intersection, the Select and ON windings are pulsed in the respective row and column desired. The coincident current sets up a particular flux path in the selected core due to the orientation of the windings and holes that switches it to a selected status. After being selected, the Select and ON currents can be removed and the core will remain selected until it is reset by a OFF pulse.

Information can then be written into the selected core and read out via the independent write, read and sense windings.

The magnetic core crosspoint switch serves a two-fold purpose. Besides acting in the conventional crosspoint switch fashion, the storage property of the magnetic core is utilized by temporarily storing the information in the selected intersection. When reading, the information arrives from the selected unit and is stored in the appropriate intersection at a rate governed by the character rate of the input device. The columns are sequentially sampled and the information read out and written into the accumulating memory. The only requirement is that the sampling of a particular column be done prior to the arrival of the next character. Because of the speed of the accumulating memory cycle which is in the range of 20 to 30 times that of the character rate of the low speed devices, this is readily accomplished. It is possible to operate several input or output devices simultaneously. The number of input and output devices operating simultaneously is governed by the necessity to service all that are currently selected within the character cycle of the input or output device with the fastest character rate.

Development of the core component is continuing to determine the number of parallel paths that can be contained in one core. A core with 7 information paths would be ideal for this purpose since a single core would serve for one intersection of the crossbar switch to handle information flow.

Because the core has the capability, with a different winding arrangement, of passing information immediately rather than storing, it is being considered in connection with the problem of controlling the input-output devices.

Reliability

The magnetic core crosspoint switch is one example of the continuing effort to assure long term reliable performance of the STRETCH computer. Some of the advantages of this type of device include:

1. No deterioration of components (except possibly drives).

2. Driving currents are not critical.

3. In contrast to a mechanical switching device, the magnetic equivalent does not require periodic service and maintenance.

4. The operating speed limitations of the device exceed by far the operating speed requirements of this application.

Choosing reliable components and employing them judiciously in the design of the machine is the first step in assuring extended uninterrupted performance. Checking, error correction and fault location are being incorporated to the greatest possible extent in the LINK Exchange. This is important since the best time to include features of this type is while the design is flexible.

Some of the considerations in these areas that are presently under investigation include the following:

1. Duplicate recording on tape to permit automatic correction of errors which could not be corrected by simply backspacing and rereading.

2. Checking of instruction interpretation and routing.

3. Checking of data transfer.

4. Checking of control signals to external units.

5. Methods of automatically locating and recording errors and faults.

6. Procedure to be followed when an error is indicated.

These and other problems of this nature are not confined to the LINK Exchange, but exist throughout the machine. Detailed examination of the LINK Exchange will give us solutions to these and many other problems yet to be encountered in the design of the complete system.

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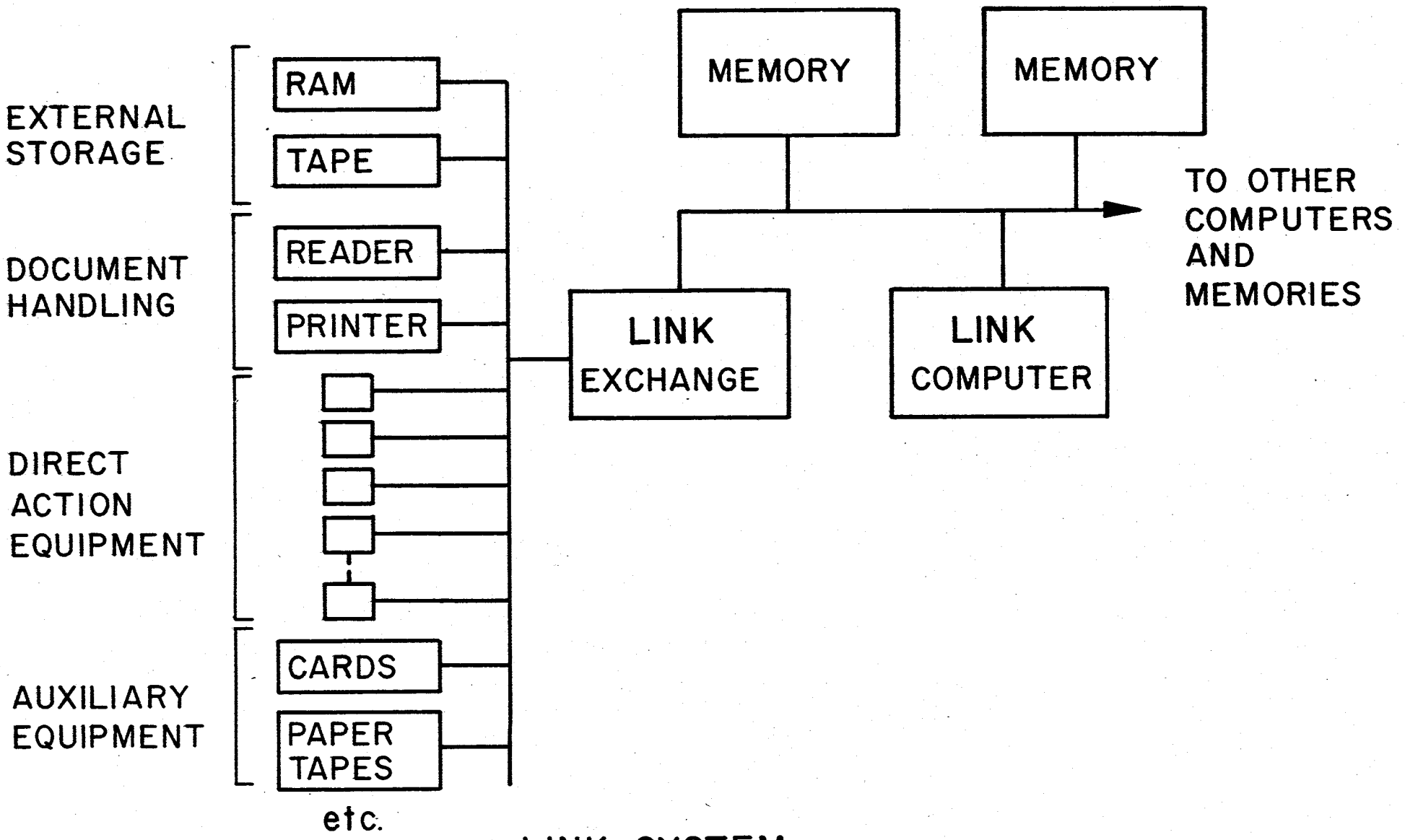
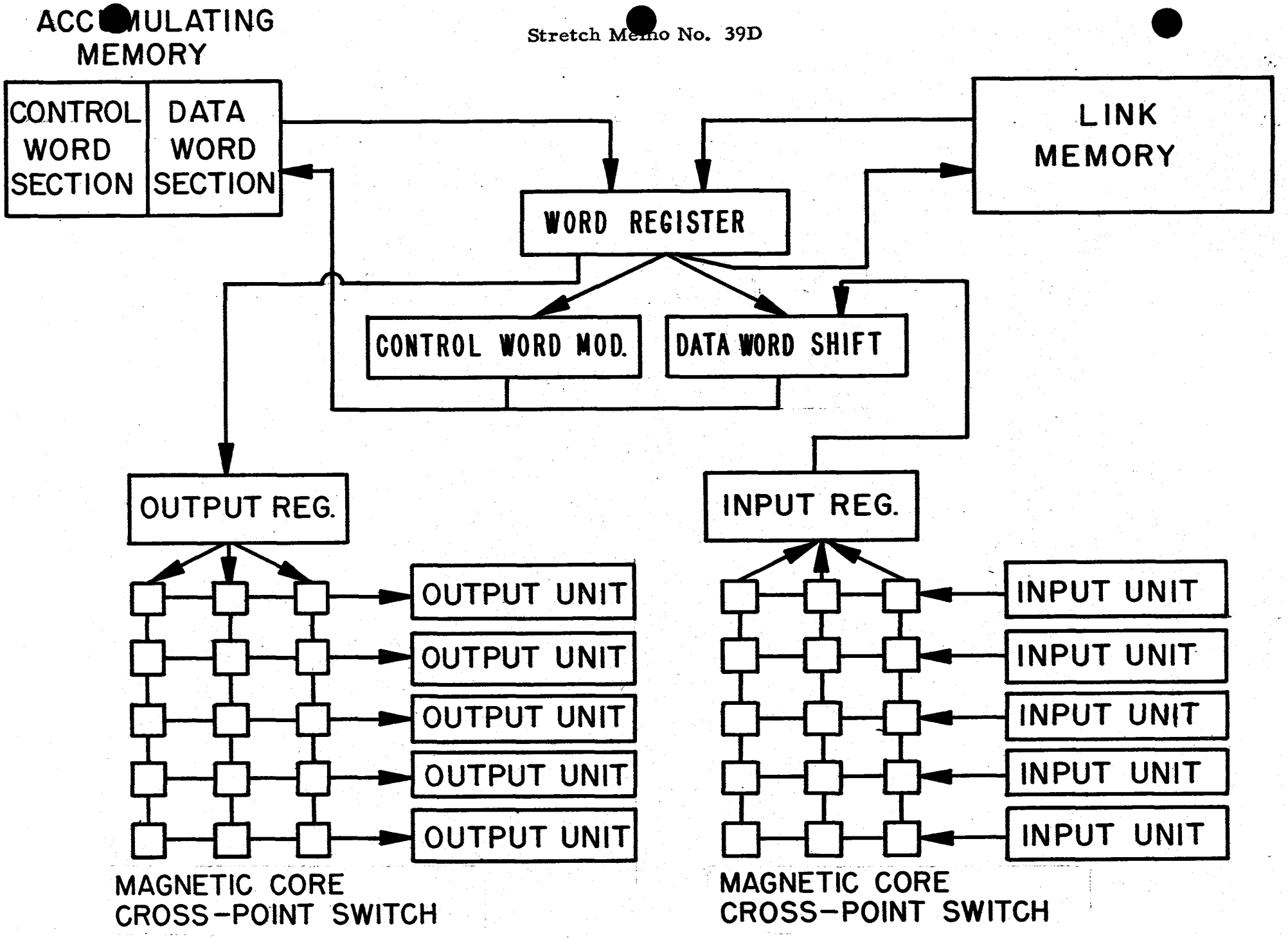
FIGURE NO. 1



LINK SYSTEM



LINK EXCHANGE INFORMATION FLOW

Figure 2

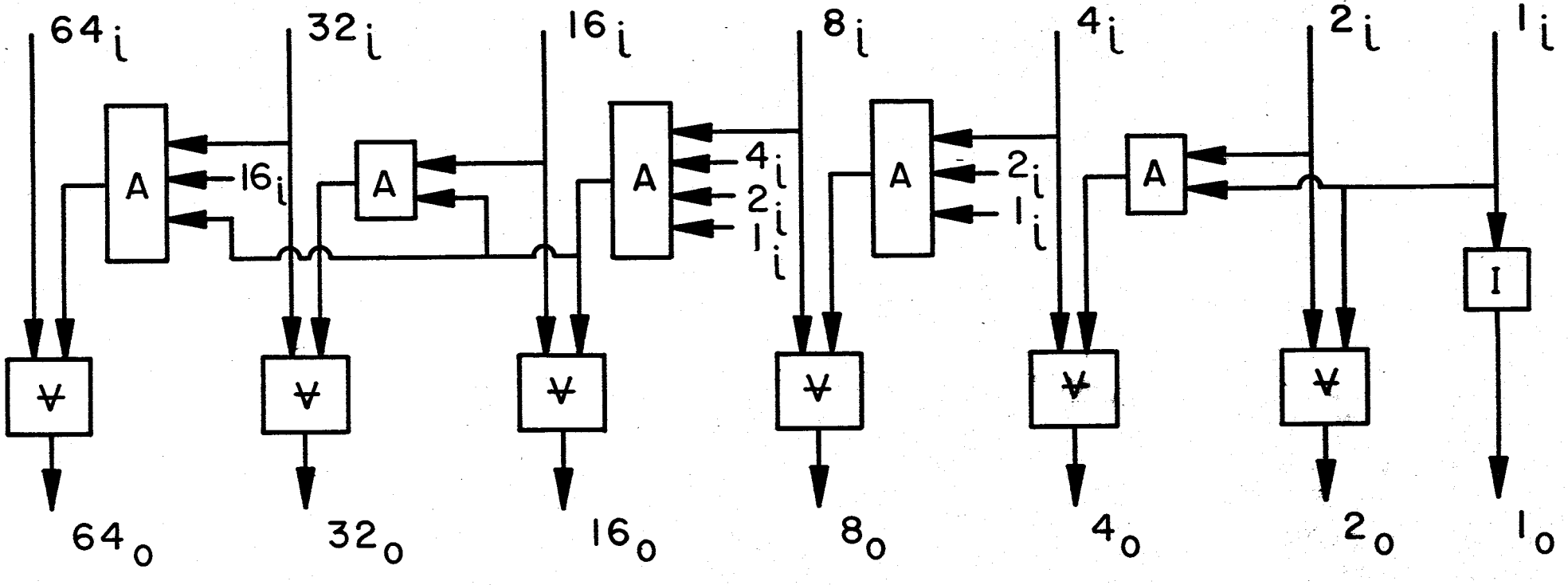
$$1_{OUT} = \overline{T}_{in}$$

$$2_o = 2_i \forall 1_i$$

$$4_o = 4_i \forall 2_i \cdot 1_i$$

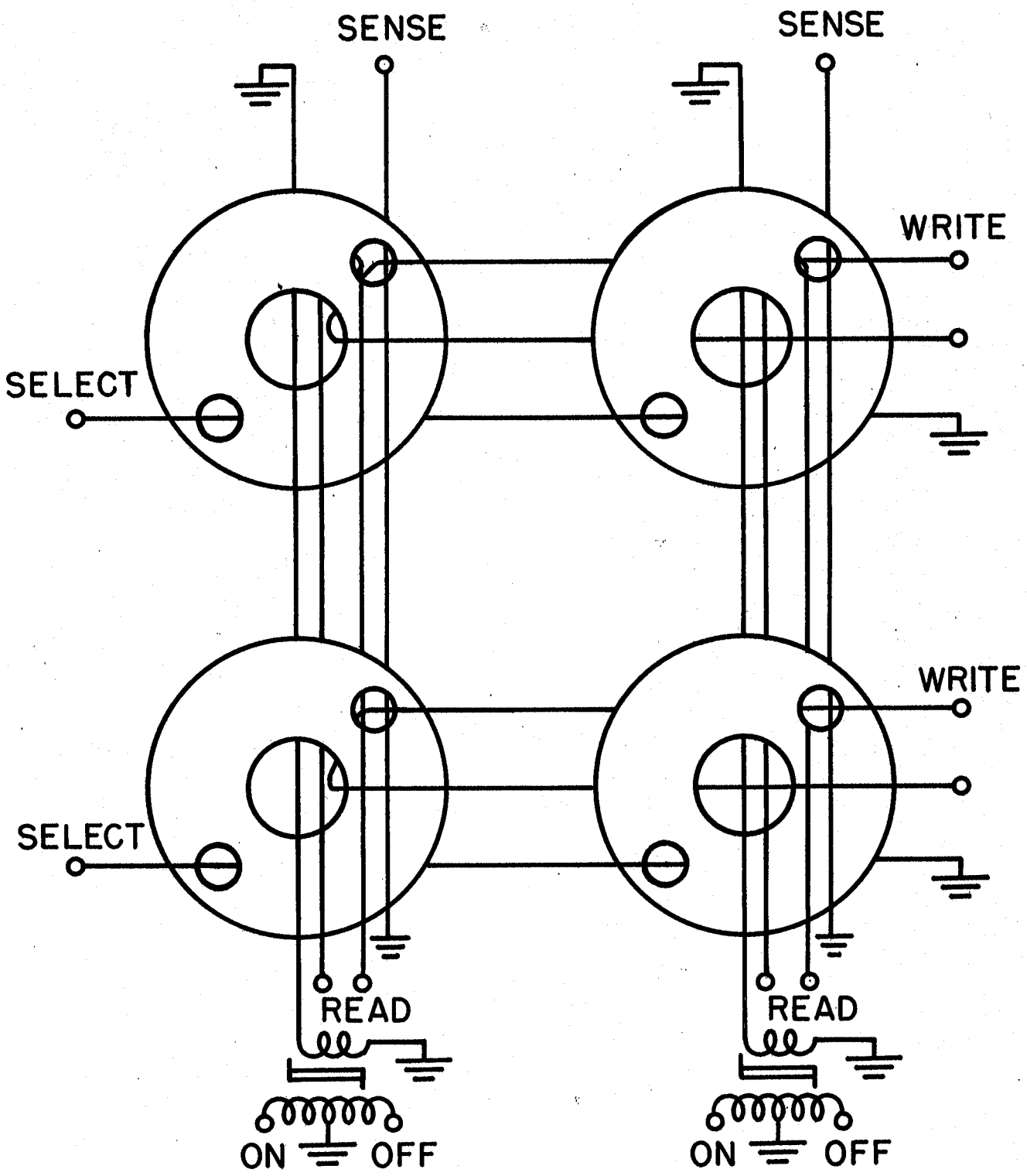
$$8_o = 8_i \forall 4_i \cdot 2_i \cdot 1_i$$

$$n_o = n_i \forall \left[(n-1)_i \cdot (n \cdot 2)_i \cdots\cdots 2_i \cdot 1_i \right]$$



STEPPING A BINARY NUMBER UP BY 1

Figure 3



MAGNETIC CORE CROSS-POINT SWITCH

Figure 4