PROJECT STRETCH

File Memo #29

SUBJECT: Stretch RAM, Initial Specification

      BY: N. P. Edwards

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        The following are the proposed specifications for the Stretch RAM. These are based on a conservative projection of the present RAM specifications. If the development exceeds these specifications, or shows definite promise of doing this, the specifications will be revised to take advantage of the increased performance.

Specifications

        1. Input and Output mode parallel transmission of a complete word and checking or auto correction information.

        2. Transmission rate 1 word, every 2 us. Read or write. Occasional blanks (ie. time when no word is transmitted) to allow for asynchronous operation...

        3. Addressing binary by 2048 word blocks, read or write.

        4. N. R. Z. recording - information must be written by the block - no selective writing within the block.

        5. Reading or writing of any number of sequential blocks with no interruption. Two independent heads and actuator mechanisms per disk side will be provided to permit sequential stepping through tracks.

        6. Revolution time approximately 17 ms.. Hence time to start reading on a selected block will vary from 0 to 17 ms.

        7. Random track selection time will be under 100 ms.

        8. Timing will be from timing track or similar device snychronized to the RAM rotation.

        9. The capacity of a single logical RAM will be at least 1,048,576 words.

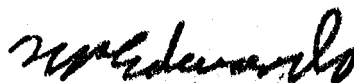Characteristics to give the above specifications:

1. RPM - 3600
2. Disk diameter - 18"
3. Disks per logical RAM - 30 to 34
4. Bits/disk side - 1,048,576
5. Bits/track - 8192
6. Tracks/disk side - 128
7. Bits/inch - about 250 maximum

Characteristics which may change, and the potential effect.

1. Increase bit density. Since this would increase the bit rate, fewer disks per word would probably be used with the full word assembled in the sync register. An increase in information flow into and out of the RAM above 1 word every 2 us. may demand too large a percentage of the memory time.

2. Increase capacity of RAM (a corollary of 1). This will merely reduce the number of RAM's required.

3. Decrease access time. Either RPM increased or actuator mechanisms for heads improved. Increased RPM will reduce re-start time but will increase data rate. (See 1 above).

N. P. Edwards