(2)

PROJECT BETA January 16, 1956

FILE MEMO # 8

SUBJECT: Delayed Store or Store Decoder

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A delayed store system could increase the efficiency of the machine by permitting the store instructions to be executed in an asynchronous non-sequential fashion with respect to the instruction sequence. The system would in theory use some of the unused time of the memories to execute the store instructions. (The delayed store could allow time for generation of error correcting parity bits. If the error correcting parity bits are generated in the store register, the problem of checking the transmission to the store register must be solved.)*

One system to effect this is described in a memorandum to B. Housman, "Some Ideas Regarding a Stretch Type Machine for the SAGE System" by W. A. Hunt, 10/20/55. A variation to this is a system where the store instruction, as it is executed from the arithmetic decoder, loads the data and the address of the memory register in which it is to be stored into a temporary storage register, from which it is stored in accordance to the philosophy of the first paragraph of this memorandum.

Some of the control problems associated with this type of operation are discussed in Stretch File Memo #15 and BETA File Memo # 9.

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* Added 3-15-56.