H. Kolsky

PRODUCT PLANNING & MARKET ANALYSIS DIVISION

IBM

MEETING OR CONTACT REPORT

70-6076-0

Project: STRETCH Mathematical Planning Meeting #6	Date of Report: June 24, 1957
Purpose of Meeting or Contact:	Date of Meeting or Contact: June 10, 11, 1957
	Reported by: D. W. Sweeney
	Dept.: 749
Place of Meeting or Contact: □ WHQ □ Phone Other:	Follow-up Date:

List Personnel Participating
Give Report (including next action)
Indicate Distribution

IBM

Mr. E. F. Codd
Mr. G. A. Blaauw
Mr. J. E. Griffith
Mr. J. Cocke
Mr. D. W. Sweeney
Mr. W. Buchholz
Mr. F. P. Brooks
Mr. W. W. Wolensky
Mr. S. W. Dunwell
Mr. F. Johnston

LASL

Mr. D. Wood
Mr. E. Voorhees
Mr. H. Kolsky
Mr. R. Lazarus
Mr. B. Carlson
Mr. M. Goldstein

Mr. Dunwell opened the meeting and introduced Mr. Mussell as the assistant manager of the Stretch program. He then reviewed the progress of the project since the last meeting. The circuits group is now out of the Stretch project and under the direction of J. C. Logue. The tape system is now under the direction of T. Vinson. Three people are now reviewing our technical position on transistor components. There are no statements about their conclusions but within a month IBM will know accurately where it stands on quantities and techniques. There is a problem of choosing among manufacturing techniques, and we must be in production for model construction. The memory program has gone as far as possible without a sufficient number of drivers. Limited arrays can be driven but we cannot simulate the transistor drivers with tubes. It isn't a question of whether it can be done, any unexpected troubles would indicate a slow down of speed not a failure. One group is proceeding with a large test assembly which will consist of two registers and an associated arithmetic device. The circuits are compatible with a wide range of transistor speeds and we will use the best we have at the time. The assembly is being laid out as the final package might be to determine the packaging.

Mr. Dunwell indicated that the Harvest Manual had been produced for Bu Ships in May. Steps are being taken to provide LASL with copies.

Mr. Dunwell then described the background of a machine organization which was to be presented. IBM has several broad areas of obligation. One is the LASL requirements, their equipment will be identical with the needs of other. Second there is the provision for the next generation of machines. Third there are the requirements of Bu Ships who have provided some of the support of the project so far. With these obligations in view, can they be met in a single program with respect to components, circuit memories, and I/O requirements?

The main question was the computer proper, are the various requirements alike or different. A committee was appointed on May 1st consisting of F. P. Brooks, W. W. Wolensky, G. A. Blaauw, J. E. Griffith, E. F. Codd, and D. W. Sweeney, to determine if IBM could produce a base machine to which additions could be made to satisfy the LASL and Bu Ships requirements. The committee's conclusions were that such a base calculator could be designed to which such additions could be made. The additions are slaves to the base and have additional, not new languages.

Mr. Brooks then presented a description of the machine system indicating the parts as B, S, and H, where B in the base computer and B+S is the LASL computer and B+H is essentially the computer described in the Harvest Manual. He indicated that the Harvest system lends itself readily to this separation. Therefore, B+H is practical. B has both versatility and flexibility with variable field length, variable byte size, all arithmetic and logical operations, and its own floating point system. The calculator is serial. S consists of the look-ahead feature and the parallel, binary, floating point device.

The presentation was followed by a long question, answer and discussion session. The comments, questions and discussion from LASL were directed mainly towards whether B+S would satisfy their requirements. The immediate reaction from LASL was that arithmetic efficiency was being sacrificed for variable length. Since the S addition had the required floating point commands, the discussion centered around indexing and the index format, pre-post store operations, and the instructions format. The question was one of whether two instruction formats, two index formats, and two indexing systems would be required to get both the variable length and parallel floating point arithmetic efficiency. Again LASL pointed out that pre and post store operations and a universal result register implied 30% to 40% savings in code lengths, and that geometric indexing was preferable to them. A specific criticism of indexing was the requirement of two instructions for modification, test, and conditional transfer on indexing. They again pointed out that the 20 bit address seemed too large, and that the instruction format was filled with fields which were not used by the floating point operations such as the bit address and field length specification.

Mr. Dunwell stated that since large memories were needed and this appears expensive could economies be effected by using variable length floating point data formats with some mechanism to compact and expand the data. Mr. Lazarus indicated there might be a format bind and asked how one could specify the length of both the exponent and mantissa and compact and expand with no time lost.

During the discussion Mr. Dunwell indicated that because of cost considerations IBM would probably go to 1024 rather than 512 word blocks for the 0.5 usec memory and 16384 rather than 8192 word blocks for the 2.0 usec memory.

Another part of the discussion centered about new methods of doing problems. LASL stated that solutions to transport and fluid dynamics problems are the bulk of their work, and the machine must execute present methods optimally without too much speculation about new methods as these aren't known yet.

Mr. Cocke then explained the program which he wrote for the 704 to simulate the look-ahead for the LASL machine and generate the timing diagrams. He explained what assumptions he made in the design of the look-ahead and indicated the parameters which could be varied so that the problem of an optimum look-ahead device could be studied. They are:

Number of look-ahead stages
Number of memory units
Timing of memory units
Arithmetic times
Bus times
Index times
Number of levels of indexing
Amount of I/O traffic.

The next day Mr. Buchholz indicated some of the changes that had taken place in the Exchange since the last meeting. The main change was the elimination of the cross-point switch in favor of direct scanning of the channels.

Mr. Carlson then presented the results which LASL had arrived at for the use of an I/O computer operating simultaneously with the main computer. He said that they used to think of the I/O computer as a bubble on the main computer but that it appeared from the B+S configuration that the I/O computer was now the main part. Assuming an I/O computer running simultaneously with the main computer but secondary to it, they felt it would have the following uses.

1. I/O radix conversions particularly floating binary to floating decimal and vice-versa.

2. Interruption buffer to the main computer to control all I/O traffic.

3. Decimal arithmetic for small problems, data analysis, and data processing.

4. Searching and sorting

5. Controlling code and data transfer from memory to memory in blocks while the main computer is busy.

In the discussion following , Mr. Buchholz indicated that IBM in its evolution of computers had originally considered something similar to B+S but at the time of the Los Alamos proposal were considering separate computers but that the philosophy was now back to the B+S configuration. A large part of the succeeding discussion concerned break-in and interrupt conditions and priorities. LASL felt that they would like priority break-in for certain I/O devices but not others so that the main job running would have highest priority and that other jobs would be kept running at the convenience of that program but would not interrupt it. The present interrupt system does not provide for this.

Mr. Carlson then spent some time going over a proposal he had made at an earlier meeting concerning indexing and addressing. This was for the benefit of some of the IBM people who had not heard it or had not understood it. He indicated that an address is equivalent to a mathematical symbol; A, B, C, etc., A is a symbol, and C (A) i. e. contents of A, is identical with the value of the symbol. Next we step to $(A, X) = f (X)$ X is now a variable or an index quantity. The next step is $(A, X_1, X_2, X_3, \ldots.) = f (X_1, X_2, X_3, \ldots.)$ and $C (A, X_1, X_2, X_3, \ldots.)$ is a function table of the dimensions $X_1, X_2, X_3, ---$. Dimension is a concept like a number, and we should generalize our specifications for indexing to include this concept. He indicated that there was certainly some waste motion in multiple indexing but this is also true of floating point and that the generality of multiple indexing allowed very straight forward programming.

Any index now becomes a variable, and it is only necessary to use one word to completely specify the variable i. e. a current value, an increment, and a limit. A discussion followed as to what the limit should be, either a count and a count limit, or a limit value. LASL still prefers having four values in an index word; value, increment, count, and count limit.

Mr. Wood made the statement that it may not be possible for LASL to compromise on instruction and index formats and there there did not seem to be the same vocabulary for variable length and floating point. LASL indicated that it might be necessary to start some discussions of a classified nature so that IBM might realize the magnitude and complexity of their problems and why LASL was so concerned about the best possible indexing and arithmetic efficiency.

Mr. Blaauw had drawn up a list of questions which had concerned the previous day's discussion. These were presented to Los Alamos with a request for comments. They are attached to the end of this report.

Mr. Dunwell then took the group on a tour. The group saw the test array for the 0.5 usec memory, some of the core elements, a driver transistor, the transistor tester, and recorder, and the frame for the test assembly for the registers and adder.

Mr. Voorhees spent some time discussing the formulation system for automatic programming which was presented at the previous meeting with J. Griffith, I. Ziller and D. Sayer in a separate group.

Mr. Sweeney indicated that the B and B+S system was the first organization of the computer which was sufficiently detailed so that evaluation could be made. He promised to send Los Alamos as detailed a write up as possible about B and B+S so that they could begin an evaluation immediately. It was agreed that in two or three weeks there should be some informal contacts to review the progress of the evaluation. Mr. Dunwell thought that more problems should be examined in detail and stated that he had not seen one complete problem from Los Alamos. Mr. Lazarus stated that he had not seen any real ideas for machine design dictated by problem examination, but that evaluation of many problems agains a machine organization was more fruitful.

It was agreed that the next formal meeting would be held early in August but that several informal contacts should be made until then.

1. Is it acceptable to have instructions of the pre-load, post-store, type apply to floating point type instructions only.

2. Is it sufficient advantage to have only multiple accumulator operation and not pre-store, post-store, pre-load operations.

3. How large should the second address be.

4. Is it acceptable to have geometric indexing for floating point operations only.

5. What is the smallest number of index registers acceptable. What is an optimum.

6. If there is a choice between geometric indexing and multiple accumulators, which is preferred.

7. Would it be desirable to address high-speed registers both as geometric indices and multiple accumulators.

8. If the operand address would not span full memory, what size of address would be acceptable.

9. On the same assumptions, what maximum index address would be desired.

10. Is it acceptable to concentrate the effort of obtaining very high-speeds upon floating point arithmetic rather than other data manipulations.

11. Is the floating point format acceptable.

    a. Mantissa 48 + 1
    b. Exponent 10 + 1
    c. Tag bits 4

12. Is a zero tag bit acceptable if it would speed up operations.

13. If it were possible to use and specify variable field length floating point operations, would this be useful.