

Meeting Tue 11.00 a T-1 Conf Room

~~GENERAL INFORMATION~~

These are suggestions only

Memory arrangement: The memory should, if at all possible, be arranged without gaps in this order, assuming at this time 20<sub>8</sub> (16) W registers, 2000 (100k) PW locations, and 100000 (32768) NW locations:

<u>Memory</u>	<u>Addresses</u>
W	0 - 17 <sub>8</sub>
PW	20 - 2017
NW	2020 - 102017

Provision should be made to increase any memory block above by changing the addresses allotted.

The W registers above are regarded as fast accumulators, 0, 1, and 2 referring to the A, B, and C arithmetic registers, respectively. An additional 16 special purpose W register of 36 bits each are required. These are addressed differently and divided into two groups, 12 index registers I<sub>1</sub>, and 4 level registers L<sub>1</sub>.

Instruction format: The following format involving an operation and four address parts is suggested:

Field →	Ope	T	X	D	P
Bit →	12	12	12	16	6

T, X, D, and P are normally to be interpreted as follows:

T Accumulators 0 - 1777<sub>8</sub>. The first two bits provide for four different interpretations of T.

X Index registers geometrically addressed, i.e., by giving a (1) in one or several of twelve different positions, each position corresponding to a register. S (X) =  $\Sigma$  C (X) summed over those X<sub>i</sub> ≠ 0. If all X<sub>i</sub> = 0 then S (X) = 0.

D the base address 0 - 177777<sub>8</sub>. The first two bits provide for four interpretations.

P these bits correspond to the P-bits in the data words. They are to be used to effect boundary type IX - instructions.

Level register L<sub>1</sub>: These registers are not referred to directly by the instructions. A level counter is associated with these registers. If a "TIL" - instruction (TK-type) is given to effect a temporary transfer to another code level (1) the level counter is increased by unity and (2) the location (I) and effective address (A') of the TIL are stored in the register corresponding to the level count:

Field →	L <sub>1</sub>	A' <sub>1</sub>
Bits →	18	18

If a "TEL" - instruction is given specifying a return to the previous level, then (1) the D-part of the TEL - address is augmented by L<sub>1</sub> prior to the transfer, and (2) the level count is decreased by one.

Index registers (X<sub>1</sub>): The format specifies two quantities, a "current value" X<sub>1</sub> = C (X<sub>1</sub>) + Δ - quantity (with sign s):

Field →	s	Δ	X <sub>1</sub>
Bits →	1	17	18

The value of X<sub>1</sub> is modified by TK-type instructions, which replace X<sub>1</sub> by X<sub>1</sub> + Δ, unless a specified condition is met in which case X<sub>1</sub> is set to zero, the initial value of X<sub>1</sub>.

The condition may be (1) a comparison with C(T), with T given in the TK - instruction, or (2) a comparison of the P-bits in the TK with those in the arithmetic unit. The latter may have been entered along with data blocks to indicate boundaries, and furnish, therefore, a means for controlling calculation loops.

Accumulators (T): The first bit is used to indicate either (0) a no pre-load or (1) a pre-load of A, in which case C (T) is sent to A before the instruction is executed.

The second bit indicates a (0) post-store of A, the result of the instruction is sent to T, or (1) a pre-store of S, C (S) to T before the operation is performed.

The combination (1,1) is interpreted as a jump and exit, the other combinations have clear meanings.

The B-address: The first bit is used to indicate that (0) B is left unchanged or (1) that B is increased by C ( $L_1$ ) before C (X) is added to form the effective address A'.

The second bit is used to indicate (0) direct or (1) indirect addressing. In the first case the base address A', as specified by the first bit, is left as the effective address. In the second, C (A') is used to form the effective address.