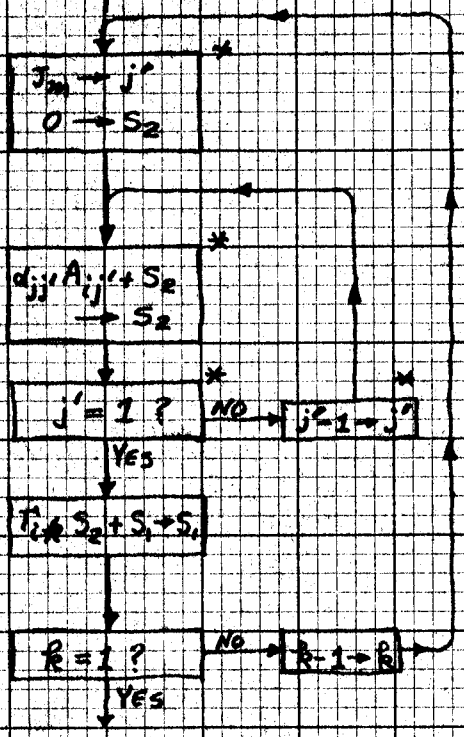
ROGERS INNER LOOPS (2) : (ONLY INNERMOST* IS CODED & TIMED.)

9/20/56



CODING

0.1_a	$J_m \rightarrow j'$	
0.2_f	$0 \rightarrow S_2$	
1.0_a	RESET ADD	α
	SUB	j
	SUB	j'
2.0_f	MPY	A
	SUB	i
	SUB	j'
3.0_a	ADD	S_2
4.0_f	STORE	S_2
5.0_a	$j'-1$ & TEST	
6.0_f	IF NOT ZERO, STORE, TR TO 1.0	

STORAGE ASSUMPTIONS:

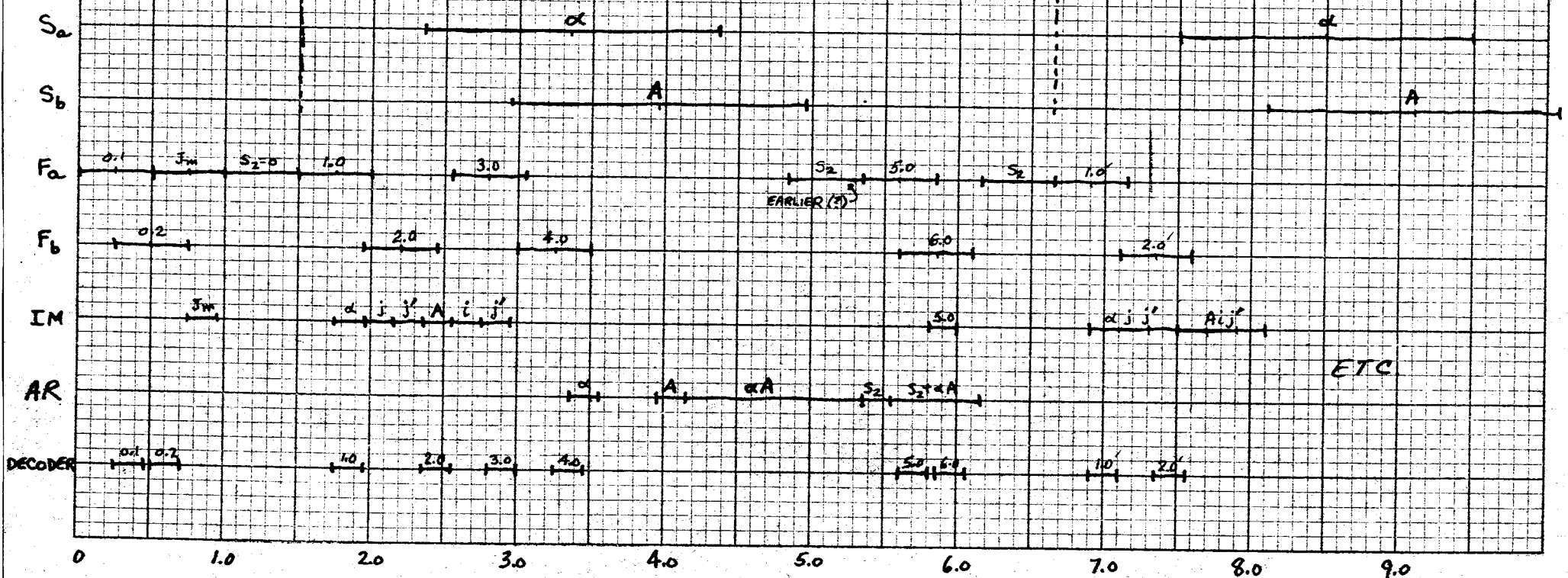
1. CODE IS IN F_a & F_f (FAST: .5 MS)
2. α's & A's STORED ALTERNATELY IN S_a & S_f (SLOW: 2 MS)
3. J_m IN F_a
4. S_2 KEPT IN EITHER F_a OR IM (depending on case)
5. j''s j_i's KEPT IN IM (INDEX MEMORY)

9/20/56

ROGER'S INNER LOOP: S_c & S_d ARE UNUSED

CASE 1 (FW INSTRS., FW DATA, S_2 STORED IN F_a)

BASIC CYCLE TIME = 5.125 μs.



9/25/56

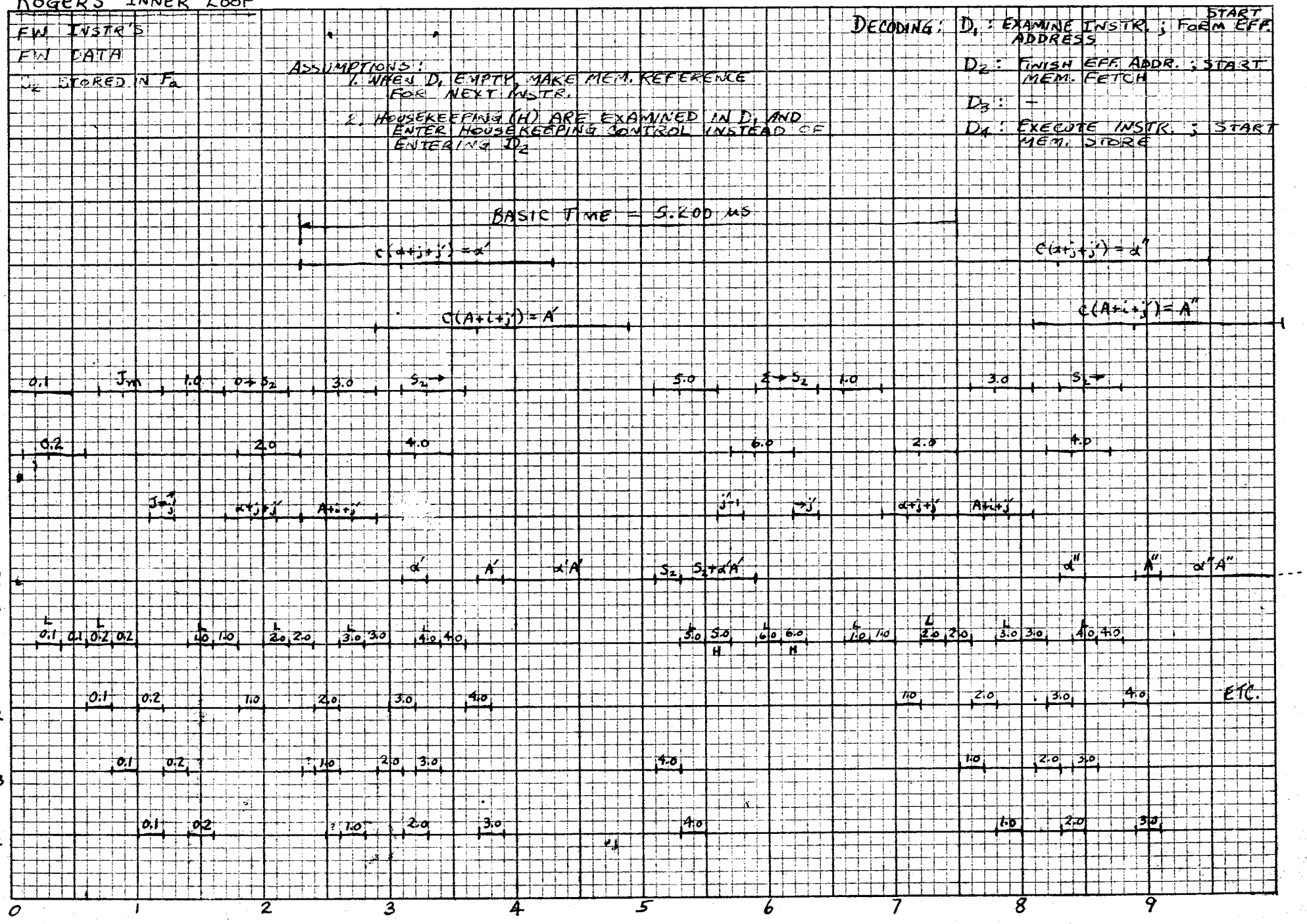
ROGER'S INNER LOOP

FW INSTR'S
FW DATA
N_2 STORED IN F_a

ASSUMPTIONS:
1. WHEN D_1 EMPTY, MAKE MEM. REFERENCE FOR NEXT INSTR.
2. HOUSEKEEPING (H) ARE EXAMINED IN D_1 AND ENTER HOUSEKEEPING CONTROL INSTEAD OF ENTERING ID_2

DECODING: D_1: EXAMINE INSTR.; FORM EFF. ADDRESS (START)
D_2: FINISH EFF. ADDR.; START MEM. FETCH
D_3: —
D_4: EXECUTE INSTR.; START MEM. STORE

BASIC TIME = 5.400 μs



ROGER'S INNER LOOP (FW INSTRS., FW DATA, S_2 IN IM)

BASIC TIME = 4.3 μ.s.

9/27/56

ASSUMPTIONS:

1. WHEN D_1 EMPTY, MAKE REFERENCE FOR NEXT INSTR.
2. IF $C(D_4) \geq .2$ μs "OLD", WHEN D_4 FIRES, $D_3 \rightarrow D_4$
3. HOUSEKEEPING INSTRS(H) ARE DISCOVERED IN D_1 AND CAN ENTER HOUSEKEEPING CONTROL (D_H) AFTER BEING IN D_1 FOR .1 μs. INSTEAD OF ENTERING D_2.

DECODER:

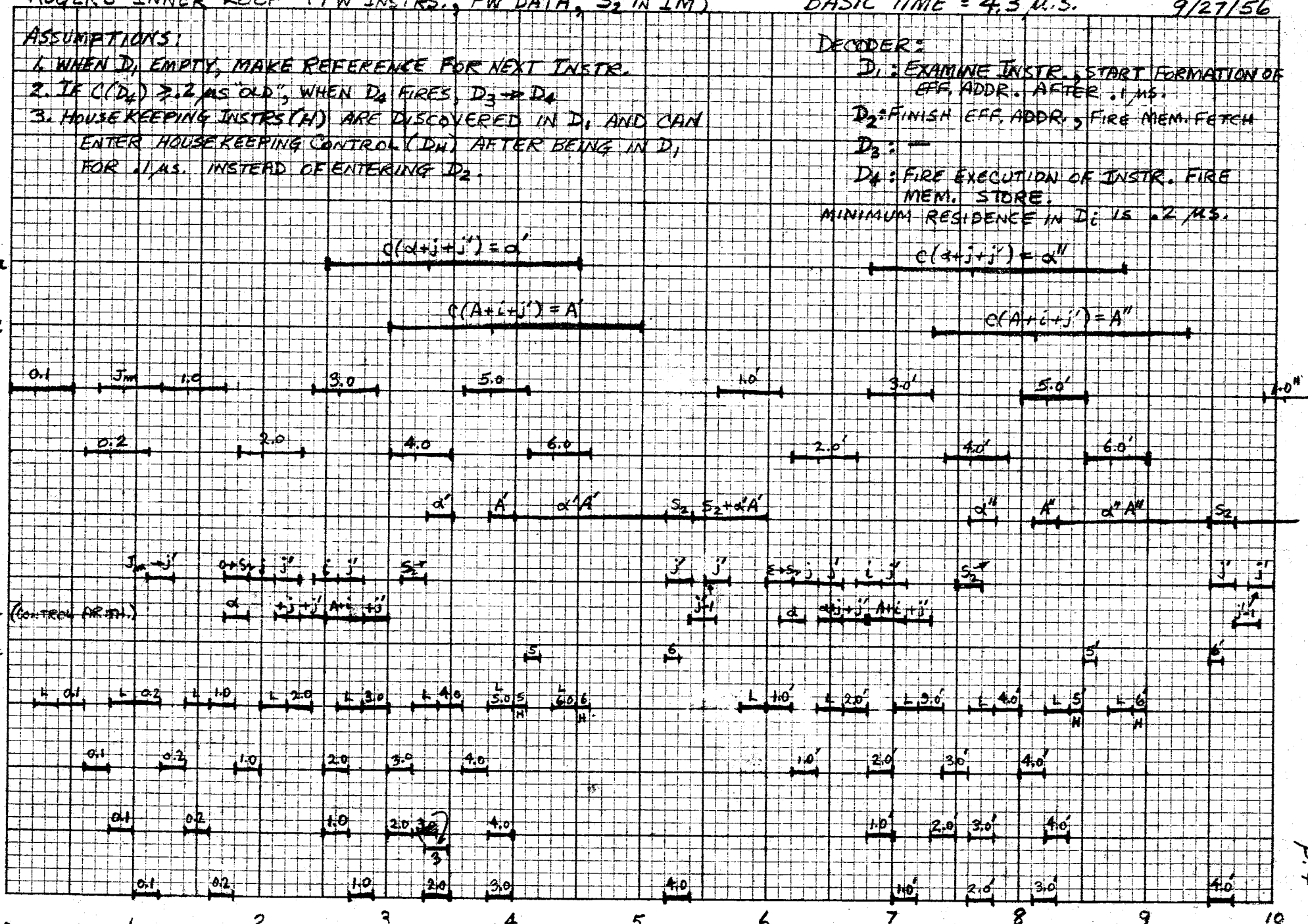
D_1: EXAMINE INSTR., START FORMATION OF EFF. ADDR. AFTER .1 μs.

D_2: FINISH EFF. ADDR., FIRE MEM. FETCH

D_3: —

D_4: FIRE EXECUTION OF INSTR. FIRE MEM. STORE.

MINIMUM RESIDENCE IN D_i IS .2 μs.



$\sum_{i=0}^{4} a_i \rightarrow Sa$ (worst case)

10/1/56

ASSUMPTIONS:
1. AFTER D_1 IS .1 μs "OLD", FIRE FOR NEXT INSTR.
2. IF $C(D_4) \geq .1\,\mu s$ "OLD", WHEN D_4 FIRES, $D_3 \rightarrow D_4$
3. "H" INSTRUCTIONS ARE RECOGNIZED IN D_1 AND CAN ENTER
4. WHEN TX DENIED, D_1 IS RESET

DECODER: D_1 - EXAM. INSTR.; START EFF. ADD.
D_2 - FINISH EFF. ADDR; FIRE MEM. FETCH (ABS ADDR .1 μs, MOD ADDR .2 μs)
D_3 -
D_4 - FIRE INSTR. EXECUTE; MEM STORE FIRE.

Sa
Sb
Sc
Sd
α_0 α_1 α_2 α_3 α_4 $\Sigma \rightarrow$ STRG.

Fa: 1.0 1.0′ 1.0″ 1.0‴ 1.0ᴵⱽ 1.0ⱽ 3.0
Fb: 0.1 J 2.0 2.0′ 2.0″ 2‴ 2ᴵⱽ 4.0
AR: α_0 $C(L)+\alpha_0$ α_1 $\alpha_1+C(L)$ α_2 $\alpha_2+C(L)$ α_3 $\alpha_3+C(L)$ α_4 $\alpha_4+C(L)$
IM
CA { AR, D_4 }
D_1
D_2
D_3
D_4
4s: 0 1 2 3 4 5 6 7 8

(TEST DENIED D_0 RESET)

CODE
0.1 J → j
1.0 ADD $\alpha_{sub\ j}$
2.0 TX 1.0 Δj
3.0 STORE (Sa)
4.0 —
WHERE Δ = 4N±1

BASIC LOOP = 1.0 μs.
ARITH = 8 μs.
EFF = 80%

P5

$\sum_{j=0}^{4} a_j \rightarrow S_a$

10/4/56

ASSUMPTIONS:
1. AFTER L, FIRE FOR NEXT INSTRUCTION
2. IF C(D4) Σ..1 μs "OLD", WHEN D4 FIRES, D3 → D4
3. "H" INSTRUCTIONS ARE RECOGNIZED IN D1 AND CAN ENTER
4. WHEN TX APPLIES, D1 IS RESET
5. A D1 REF. TO IM(i) MAY NOT FIRE UNTIL REFS TO IM(i) FROM PREVIOUS INSTRUCTIONS HAVE BEEN COMPLETED.

DECODER: D1 - EXAM. INSTR.; START. EFF. ADD.
D2 - FINISH EFF. ADDR.; FIRE MEM. FETCH (ABS ADDR .1μs.; MOD. ADDR .2μs.)
D3
D4 - FIRE INSTR. EXECUTE; MEM STORE FIRE(.1)

Sa
Sb
Sc
Sd
Fa
Fb
AR
IM
CA (AR, DH)
D1
D2
D3
D4
μs 0 1 2 3 4 5 6 7 8 9 D.B.

CODE
0.1 J → j
1.0 ADD (SUB) α_j
2.0 TX 1.0 Δ_j
3.0 STORE (S_a)
4.0 →
WHERE $\Delta = 4N \pm 1$

BASIC LOOP = 1.3 μs
ARITH. = .8 μs
EFF. = 61.5%