Meeting with IBM
at Los alamos

March 14, 1956

Black	Stringfellow
goldstein	Evans
Woods	Dunwell
Lazarus	Johnson
B. Carlson	Edwards
Kolsky	Griffith
Voorhees	Hurd
Metropolis	Thomas.

(Hurd) 3rd generation of machine 600; 700;

10 Megapulse – well balanced machine

– core

– disk 15,000,000 bit/sec

– high reliability required,

– modular construction for adding parts later.

– want to discuss future developments – extra equip.

F. Dunwell : Project Manager

– diagrams of machine (see manual)

– need some gen type of probs in mind during design

– also want to make complex decisions – "shape recognition"

Multiplexing – basic principle.

versatile input-output – communicates with other devices,

incl. real-time devices.

can do secondary conversions, etc. along with major job.

$8\times60\times60\times10^6$
$(8)(3.6\times10^{3+6})$
28.8×10^{10}

- performance level — uninterrupted operation.
"unattended" means personal intervention not needed.
- det. & corr. of errors.
→ (under 20% of hardware is checking equip.)
auto error correction — make higher speeds possible —
much larger memories will be feasible without error corr.

draw line at what can be done confidently — may do better.
- don't have production line for 10 MP transistors lower bound,
0.5 μs cores

Radix: earlier proposed decimal, now proposed binary.
- real time operations favor binary
- mapping, table-lookup - binary has def. advantages.
- logical reasons.
- equip. reasons.
60 bits. - divisible by 1, 2, 3, 4, 5, 6, 10, 12, 15, 20, 30

- Size of Mem. set by transmission line effect (Modules)

→ ultra fast mem either Transistors or very fast cores? { 2D memory not 3D small array
? This is synchronous with data unit.
- mem up to 1,000,000 wds. — divided in any way,
ultra fast | fast | Main Mem | size can be changed

External Mem.

Mag. Disk Mem:

Arith unit:

- goal fastest possible with computs.

fix. add & carry } 0.1 μs
switching } 0.2 μs

fl. add-sub 0.6 μs incl. shifting, etc.

Mpy 1.2

Div. 1.8

Str. & transfer of data word between registers, incl. J & K registers 0.2 μs

Control decoder:

- addr. modification
- look ahead of arith. unit

Input-output:

includ dec-bin & inv versa.

→ serial arith. unit

mil. shave result in mpy, etc.

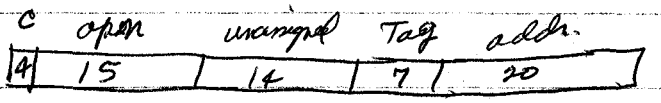
Interchange registers? no, depends on no. of in-out machines.
1 word registers (no, not chosen now)
need pair for high speed tapes.

Telephone switching practice to assign registers to I-O. unit.

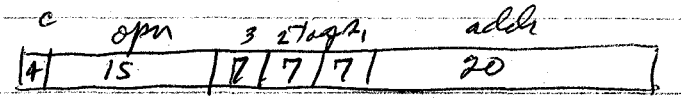
(Griffeth) : Head Product Planning experts.

Format Samples for coders:

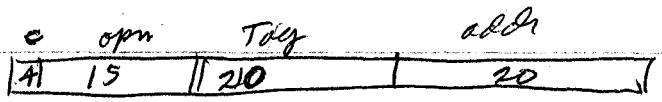
1 Basic



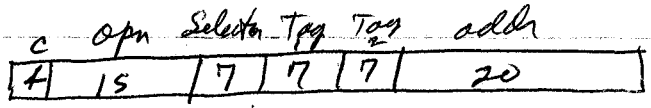
2. Triple Indexing



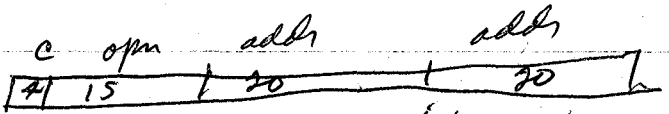
3. Full Mem. Indexing



4 Selector Inhibiting



5. Double addr



(a) for conditional transfers

(b) for unconditional returns.

Possible Opn. Classes:

(a) Primary & Sec. Arith.

(b) Floating or Fixed Mode

(c) Norm. or Unnormalized

(d) Binary or Decimal Data

(e) Direct, Indirect, Immediate address.

Baecus has looked at this for data coding

(1) Concrete terms (eg. add ∝ 201 type)

(2) Abstract (eg. add ∝ tag ; symbolic progs)

Meaning of Instr:

(a) Disassociated instr — has meaning by itself { means longer dictionary easier coding

(b) associated: depends on what has gone before { smaller dictionary harder debugging

[Ref: Bob Creel (RCA) study of telephone conversations; only 400 words 95% of Time]

new orders:

1, Table-look-up.

2, selectors (logical commands)

1, Example Table-look up: Speed: limited by Memory Speed,

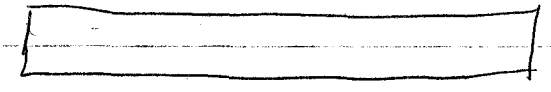
~~Binary~~ decimal to binary conv.

Instr "Transform" (size of char.) (To) (Index) (no. characters to be converted)

6 bit

look up binary equiv (small pieces)
adds directly into register
then go to next group of bits
~~End~~ index.

To + 2



2. Example of printing format. (page 7.2)

need starting address for initial nos.

" " " converted nos.

convert 4 bit characters to 6 bit characters.

no. of words is not conserved.

{ not check for validity of code eg 6 → 4 bit.
must be programmed

multiple precision:

are double precision mixed in but commands for coding it easily should be incl

I.O. computer must be able to convert word in 667 μs
ie about speed of 704

question of floating binary → fl. decimal.

Example Problem

2-D Hydro
50 × 50 Mesh 32,500 wds
(13 wds/pt)

Two passes per time step

both passes

addr. calc. 14.4 μs

Total Compute Time 75.6 μs

Total Main Mem Time 104.0 μs

154.0 μs if done straight

question of 0.2 μs access time?

may be covered later but we should consider these

Actual Time = 94.0 μs

efficiency $\frac{75.6}{94.0}$ = 80.4% (3 level decoder)

$\frac{75.6}{86.3}$ = 87.5% (4 level)

$\frac{75.6}{81.3}$ = 93% (Recode incl 4 level)

– Timing chart – can machine draw one?
can assembly prog. do anything about chart after drawn,

Floyd Johnson: Selectors

Electronic: May be turned on or off
60 set by program
console lites & stops
single 4 group tests
parallel Tr on
" Tr off
" set on
" set off clear whole group,

10 set by console sw.
8 sign – zero test
~~8 sign sw~~
2 comparisons – control
2 exp. limits
3 Overflow
8 I/O conditions

use mask: look at selectors in which there is a bit.
can one set either by prog. or by hand?
can draw off setting of all 60

Logical Connectives:

all 16 basic 2 trivial. (all 0's or all 1's)

ands, ors, incl, exclusive, etc.

for any 60 bits (either selectors or any word)

Example: Logical Transfer

let ϕ = and

1 = and

2 = or

3 = F and (not-and) "not y and -"

4 = F or (not-or) "not y or -"

Test $A\bar{B}$ (or) $\vee$ $AB\bar{C}$ (or) $\vee$ $\bar{A}C$. logical expression.

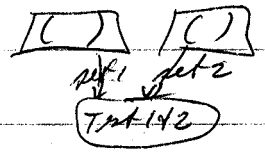
then

A1, B4, A1, B1, C4, A3, Cϕ

Test each until truth or ϕ are reached.

A, B, C, can be selectors, 1 bit

- note no parentheses included can program



Bob Evans : charge of group on input-output ..
contract negotiations

727 tape 75"/min { will be transistorized — more reliable same characters as 704

RAM disk : 2^{20} words

dia
9.7"
0.4"

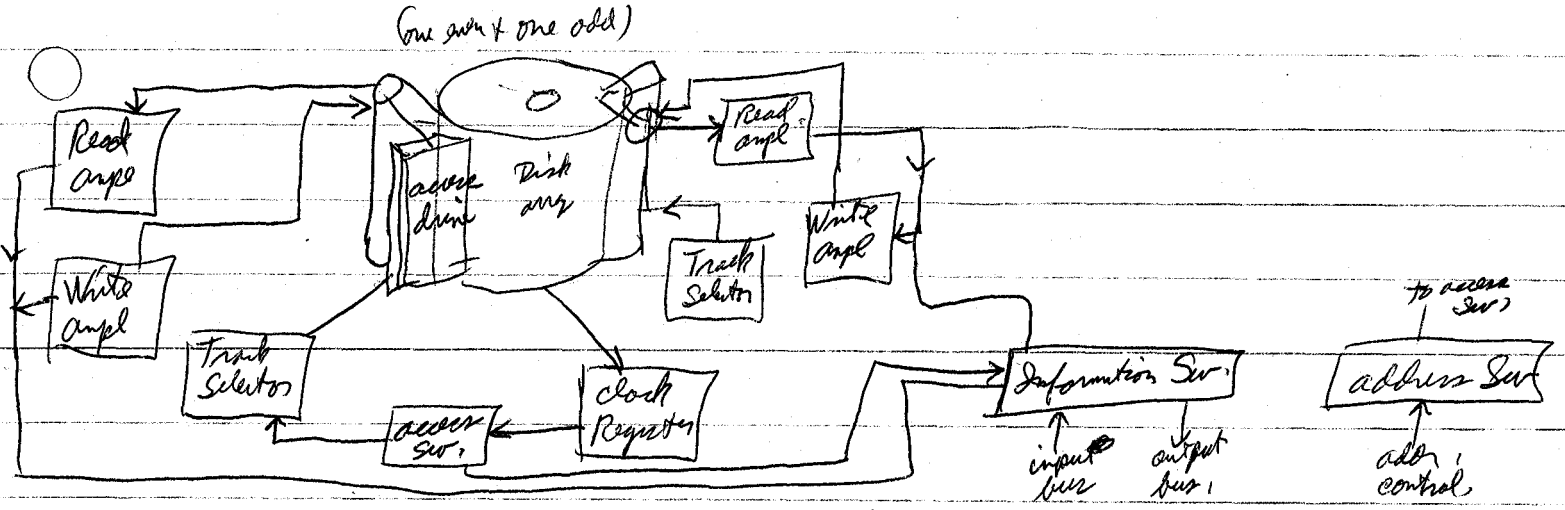
BPI = 200 bits/inch 25 mil between tracks

24" disks each side

60 heads.

8192 words around disk on certain radius

1,800 rpm = 30 rps $33\frac{1}{3}$ ms/rev



10 ms Removal of detent (last add)

0 — 200 ms nominal } 100 ms displacement time ← may be reducible to 50 ms.

10 ms Transient vibes. Time

25 ms detent latch time

145 ms

−15 ms overlap

130 ms Net overall R.A. Time

block read of 8192 words. max. on one head can read & one write

uses tape type characters.
(6 bit + 1 check)

Printer: mechanical Type 731

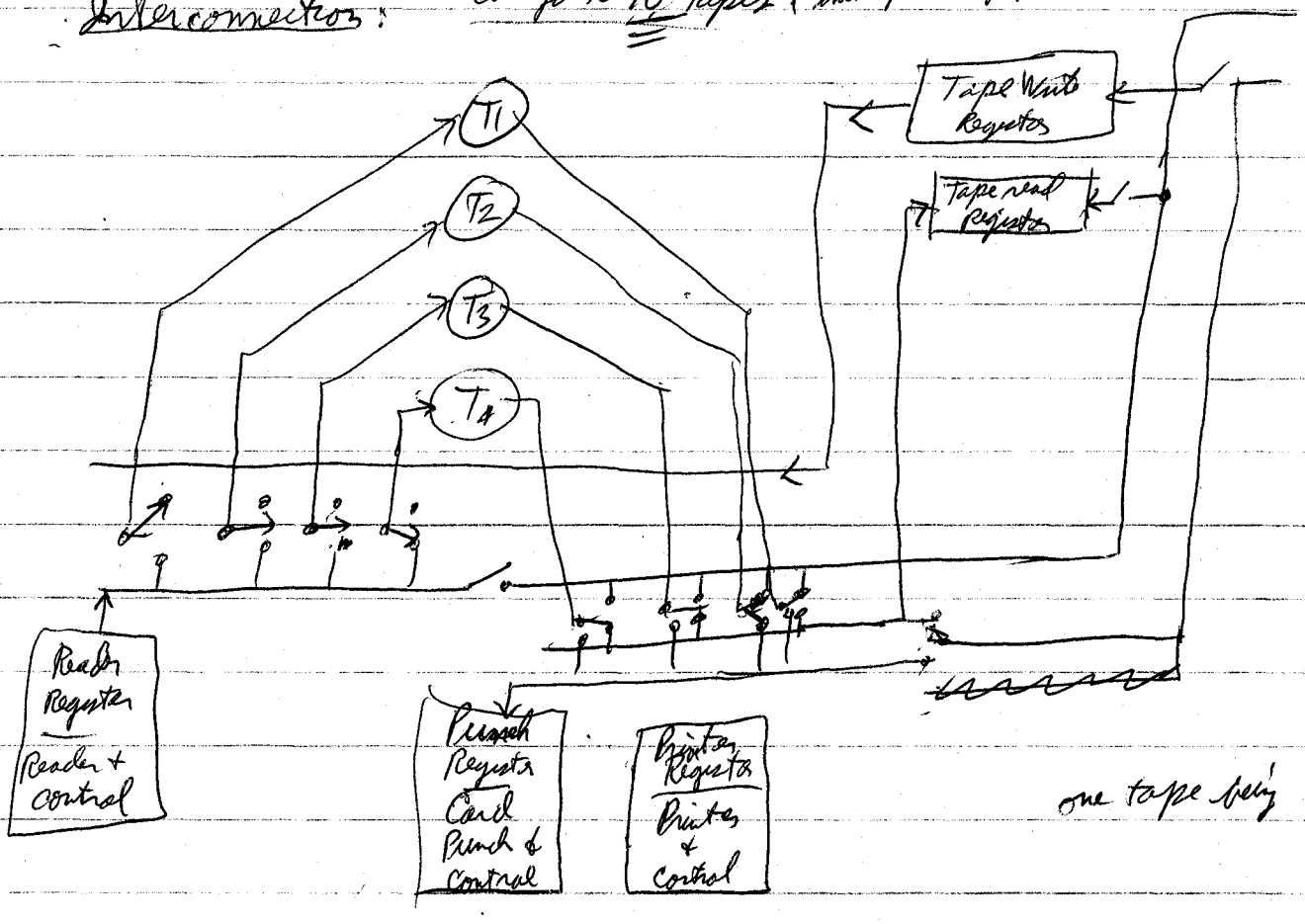
— a line buffer provided

Punch: — also has card buffers, card image buffer,
might have 10 k pulse — intermediate buffer or not. — don't know yet.

Card reader — buffer also.

Typewriter #868, word buffer

Interconnection: can go to 10 tapes, with present equip.



one tape bay

Possible Optional equip:

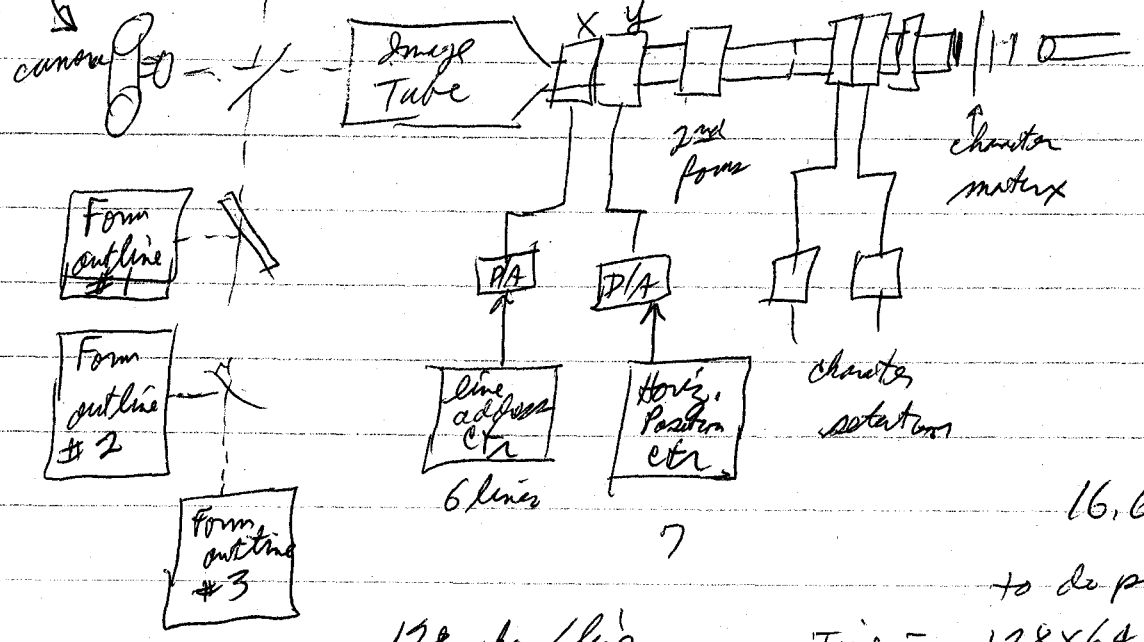
PCA Image selector 64 characters,

print at 60 μs/character

at least 5 frames/sec.

(35 mm film) → camera → NOG monitoring Tube that it is working – character check & position check

RCA Image Selector Tube:



16.6 Kc.

to do page

Time = 128 × 64 × 60 μs

128 char/line

64 lines/page

19,200. lines/min

57,600.

Printing Mode – fixed format

Plotting Mode – 1024 × 1024 points

film "Lixagraph 600" ?

5 frames/sec – may go to 15/sec.

100 ma exposure

may have self develop & viewing equip.

may have xerographic – dry printing – thermal process. some day –

RAM: 250 kbit/inch other perhaps go to high density

3600 rpm may be possible (60 rps 16.6 msec/rev)

Card punch: Likely to go faster

" reader 1000 c/m or more.

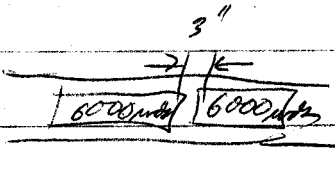
- character sensing machine:
  - 470 characters/sec being done now.
  - possible use in auto programing?

{ typewriter characters.
{ numeric & some special characters,
printed black on IBM cards.

- larger memory:
  - ferroelectric program BaTi, etc. being worked on
  - 10^6 words, etc. at comparable speeds.

- high speed tape:
  - experimental prog. indicates possible:
    1. Velocity 300"/sec
    2. Density 1000 bits/inch useful info.
    3. Reel 1200"
    4. Tracks 30 info + Auto correction
    5. Start-Stop 10 ms
    6. Record gap 3" wide tape? (or 2")
    7. Back up Time 40 ms

500 wds/in
for 80% tape ~~utilization~~ of tape surface.
(a) 6000 wds/block would be read or write.
(b) 6.7 μS/wd
(c) 7.2×10^6 wds/reel



STRETCH 50¢ per sec. cost

Nate Edwards: Engineering Details --

limitations in components,

- for one tube --- limited eventually by transmission down coaxes,

Reliability Figures

EDPM replacements/1000 hours (failures + anticipated failures)

Tubes 0.4 %

diodes 0.2 %

SAGE AN/FSQ-7 (XD-1) Jan '59 mainframe

25,000. Tubes 0.17 %

75,000. Diodes 0.13 %

300,000. resistors 0.003 % depos. carbons,

% useful assigned Time 95.6 %

Ave. Time without error 6. hr

Longest Run w/o error 49.5 hr

-- 110. operators viewing scopes etc

fix mpy ~~$3/sec~~ (16 bits)

701 [redacted]
Tubes 4000,
diodes 14000,

Question - answer period:

1,2- Signed Exponent

ov. tag ? - trial cases, one method, -

shift operation? IBM doesn't want 2nd + 3rd.

change in cost & error { 1. more features in proposal
2. know more about true cost now.

- { can give reduction estimates in two weeks from today

additional features - can't do as soon.

- 1 disk unit

- auto corrections

Mechanical Printer : $4,300 per mo rental.

Peripheral equipment :

2nd meeting Mar 15:

(Nate Edwards)

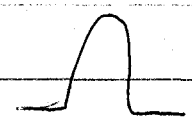
Components: Present Status

Philosophy: 3½ yrs from now - best possible then -

High Speed Transistors:

→ Are now { 5 m μsec pulse duration } feeding into few hundred ohms - experimental Transistors

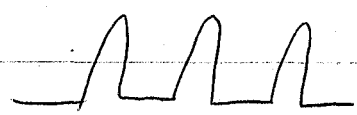
These are good enough - better than needed

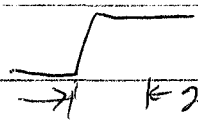
put in  came out - with gain { voltage - excess of 40 volts.

5mμsec

(sine wave ~ 300 Mc or more)

Some have run up to 14 Megapulse ir

Def: can count at 0.1 μsec. 

infers 

→| |← 20 m μs

Total no. of Transistors over 20,000. ? rough guess.

IBM will be in assembly line on slow transistors by end of this year.

has taken year to get pilot group in factory.

Slow transistors now thru pilot plant (100 kpulse to 200 kpulse Transistors for 608, (10 Mc Standard nomenclature

~37-39% good yield transistors

alloy junction type

considerably more than 300 per day,

Memory drive power transistors,

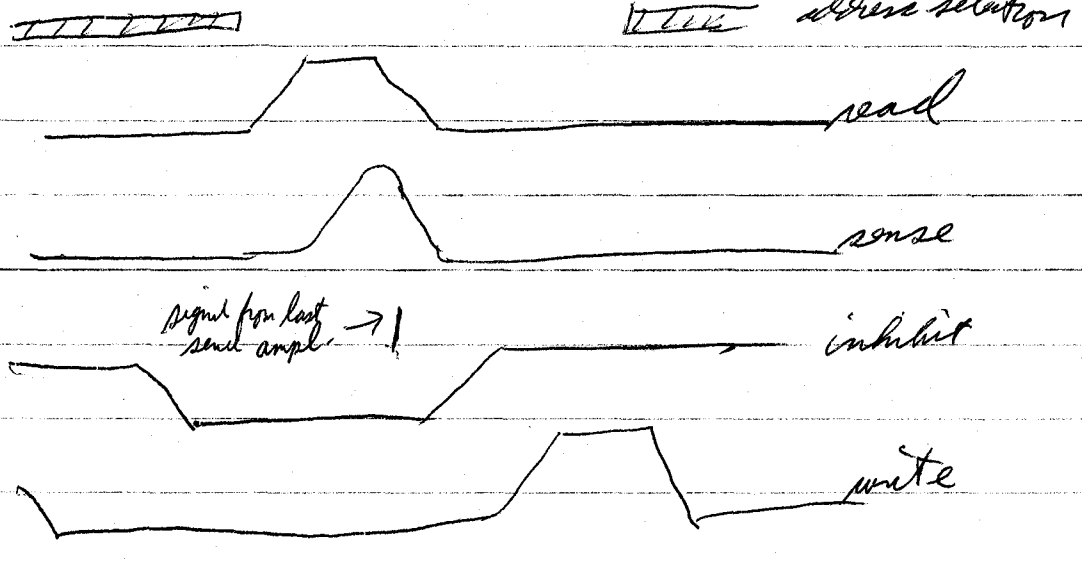
- Xp. work on

have gone to 7 m/μs 200 ma pulse without heat sink.

Philco Motorola, BTL Experimental are working on this kind of high freq. - mostly for small signal and not over drivers Type needed for computer work.

Fast Mem. Timing

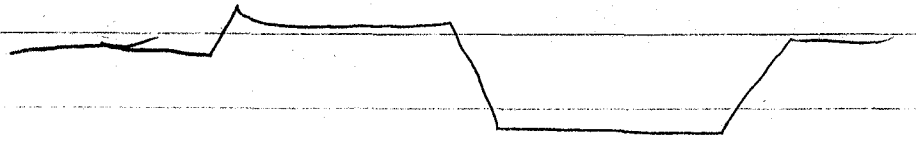
0 0.1 0.2 0.3 0.4 0.5



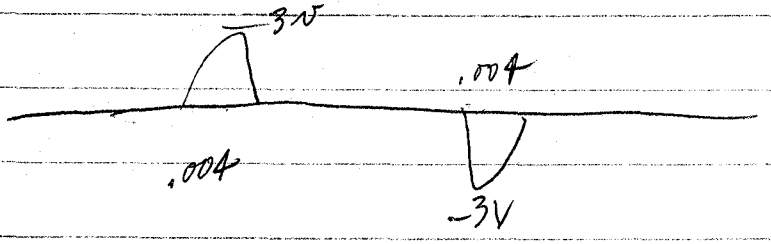
Cores: (half μs)

2 amp turn current

.002



measurements have been made on



working with isolated sections with few neighbors
- this has proved to be OK, with other memories

have made test array of several hundred
- have cut them out with ultrasonic cutter
- now computing opt. configuration.
- also doing

2 μsec mem: - could make right now if were willing to drive with high current.
- hope to go to lower current & larger cores for mechanical strength

(Same cores by 50 mil × 90 mil)

line impedance ~ 150 ohms

2 μsec on Standard coincident current type.

738 for 32,000 mem. - have made transistors on 4μs. basis cycle in 9 μs for 705 mem.

→ Possible difficulties for ½ μs core which may come up
1. Energy losses in core
2. very good wiring techniques - may have trouble with high dI/dt

diffuse transistors — high voltage up to 100 volts

evaporated film — have backup proj going for either 2 μs, ½ μs.

There are no outside distance type components.

Arith Unit:

complete add in 0.1 μs including carrys. done at same time.

Ref: Trans. Comp Sect IRE Panarine (?) — similar work.

exact method hasn't been chosen — collapse of carry on statistical method. — ?

Mpy: how many adders.

- possibly take 4 bits at a time — takes 12 pulse times instead of 48.

using 4 × 4 matrix. to add. (can skip zeros.)

Div: — analog of Mpy in circ.

sq root? haven't looked at.

Subtract gate/plate 4 bits at a time.

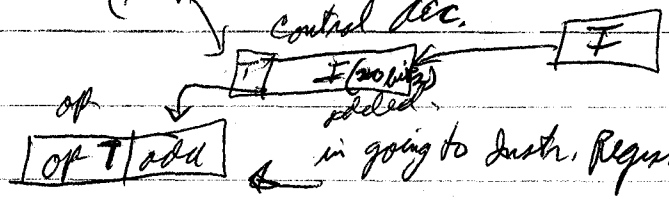
of Mpy

Exact method depends on components.

(to avoid ref to mem)

(Griffith) Control Operations:

op T add



Control Ac. (20 bit adder)

T	N	C

for Two tags add T_1 & T_2 both slower does one at a time

question of 32 or 64 ultra fast registers,

Our Present experience: 5 or 6 index reg, 10-12 Temp. storage,

question of radix — depends of freq. of shifts

Decoding:

- partly direct operation
- partly

Money:

$3000 per mo each card to tape, tape to printer, etc.

→ switching gear makes

with slow punch $1800 or not incl 727
& control unit

slow card reader $2200

- also takes space to have other equipment

STRETCH: - must be compact maybe?

Total Est now $10. M (new features not separated out)

last summer est $7 M - (Chalf $3.5 M)

We would like xtra 1. electronic printer
2. 32 fast registers
3. another RAM maybe
4. 10 tapes

IBM Dir interested in programming research.
- would like 10 people working for 2 yrs or so -