STRETCH ARITHMETIC

Registers: The operands are in S and A and the result is formed in the adder and other circuitry and then sent to A. The adder is assumed to be effectively of double length (88 bits).

	10	44	44	Add	Mpy	Div	
S	σ, e_S & s	m_S	m'_S	Augend	Mplr	Divd	Rdr (Div)
A	σ, e_A & s	m_A	m'_A	Addend	Mplcd	Divr	Result
B	σ, e_B & s	m_B	m'_B	Previous A			

General Floating point steps:

1) Send A to B
2) Position the mantissas in S and A and form the (S op A) exponent.
3) Form the (S op A) mantissa.
4) Position the (S op A) mantissa and adjust the exponent.
5) Examine the result for exceptions.

Principal operations: We have Load to and Store from any of the registers (the first 54 bits) with or without clearing the last 44 bits. We have, similarly, Load to and Store from (σ, e_S & s, m'_S) etc., where the Store should subtract 44 from e_S and be able to detect zero exceptions. We have FA, FAU, FS, FSU, FM, and FD in single precision, the first four involving all bits of the operands to yield a double precision result, FM taking the two single precision operands (after Step 2) to give a double precision result, and FD giving a single precision quotient and a remainder.
All operations have four-way sign control, the arithmetic ones on either S or A. The above instructions make double precision calculations quite easy. With a double-length adder, however, one could consider having direct double precision instructions. Higher order precision should be made possible but no special effort should be expended to make it easy.

Step 2:

Addition: Form $p = e_S - e_A$. If p is + shift A right by p and set $e_A = e_S + 1$, if p is - shift S and set $e_A = e_A + 1$.

Multiplication: If no or only one mantissa has lead zeroes, set $e_A = e_S + e_A$. If both have lead zeroes form Z, the number of zeroes in the mantissa with least zeroes, shift that mantissa Z to the left and set $e_A = e_S + e_A - Z$.

Division: If the divisor has Z lead zeroes shift it Z to the left and set $e_A = e_S - e_A + 1 - Z$. If Z = 0 no shift.

Step 3: Schematic illustrations of Add, Mpy, and Div with 6 bit mantissas.

Add:	S	.011011
	A	.001001
	A	.0100100
Mpy:	S	.100100
	A	.110100
		110100
		110100
	A	.0111010100
Div:	S	.110000
	A	.100000
	A	.110000

Step 4: The result mantissa is shifted one step to the left and one is subtracted from e_A if a lead zero is present in the mantissa on FAU, FSU, FM, and FD. In FA and FS this step normalizes the result.

Fixed point arithmetic: To enable the programmer to set his own binary points a position-instruction is required where C (A), A being the address in the instruction, has the exponent desired. This instruction does not alter the value of the number. If the positioning is not, or only partly, possible one may want a trigger to signal this fact.