Delapenha House
Poughkeepsie, N. Y.
October 31, 1960

Ad - Hoc ITL Meeting on Super-Stretch

October 27, 1960

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Attending:

E. N. Adams, Research
G. M. Amdahl, Research
F. P. Brooks, Jr., DSD
W. Buchholz, CHQ
S. G. Campbell, DSD
D. J. Crawford, DSD Components
R. J. Cypser, FSD
S. W. Dunwell, DSD
R. A. Henle, DSD Components
E. V. Hofler, FSD
W. B. Ittner III, Research
M. Klein, DSD Components
H. G. Kolsky, FSD HQ
C. J. Kraus, FSD
A. L. Leiner, Research
R. E. Merwin, DSD
E. W. Pugh, Research
J. L. Walsh, DSD Components

An informal meeting was held to bring together key technical people from various divisions concerned with the very large computer area, for the purpose of reporting on recent developments and formulating some conclusions and recommendations to the Corporation.

A. L. Leiner reported on a Research study proposal made to the AEC (not Livermore); AEC reaction is expected shortly. Money for building a machine is not likely to come forth at this time. E. N. Adams thought that ARPA may be a better place to look for funds than the AEC.

S. W. Dunwell briefly reported on Stretch. Present technology permits building a machine of Stretch performance for half the number of components. There have been requests for multiple-computer systems.

F. P. Brooks indicated that current DSD planning was concerned exclusively with machines well below Stretch in performance.

J. L. Walsh reported on Esaki diode - transistor circuits which look promising for 1 nsec delay time. Considerable work is needed on packaging and fabrication.

D. J. Crawford outlined the work of the advanced memory group. Their target for a 2 cores-per-bit, high-speed memory is a 100 nsec cycle with 1000 words of 72 bits. There is little hope of pushing ferrites farther, but speed may be extended with metallic films deposited on glass rods. For still higher speed one needs to use flat film techniques (Zurich Research) or Esaki diodes (DSD). DSD has a 16 word Esaki diode memory working at 150 n sec, which may be upgraded to 50 n sec next year.

E. W. Pugh indicated that the Zurich target is a 50 word, 50 bit thin film memory at under 100 n sec within one year.

M. Klein reported the device group's feeling that packaging and fabrication of a 1.5 Kmc (cut-off-frequency) transistor is feasible. They are working on lower-cost packaging by surface passivation. IBM still seems to be ahead in the core driver area.

R. A. Henle indicated that the efforts of the DSD Component area would now be redirected towards lower cost components with less emphasis on high speed.

W. B. Ittner and A. L. Leiner reported on cryogenics. FSD Kingston has had success with a relatively slow (3 - 4 μsec) cryogenic memory model. No high-speed circuits have been built, but the feasibility stage should be reached by next June. One can clearly postulate speeds as high as 1 n sec, but high power limits the number of circuits for a given amount of refrigeration. It now seems as if we should have concentrated more on miniaturization. Compared with the Esaki diode approach, cryogenics ultimately promises similar speeds at less cost, but large memories at reasonable cost present a real problem.

E. N. Adams pointed out that technological trends clearly indicate the desirability of using distributed small fast memories, if only to solve the problem of propagation delays between units of large size. The group felt, however, that we know very little about how to organize and program such a machine to gain the desired performance, and this is now a key technical problem. Neither do we know how to use exotic memories with built-in logic, which have been proposed to offset cost.

Several comments were made on competitive effort in the memory area. Ramo-Wooldridge is supposedly working on construction techniques for a 1 to 10 million word memory. Remington Rand is talking about a 1000 word, 50 n sec thin film memory, but they apparently exclude the sense and regeneration loops in their statements on feasibility. Rome AFB is asking for

R & D work on a 1 billion bit memory. A member of Lincoln Labs, has commented that thin films have not yet reached the development stage, but they seem to be heading for big cheap memories, which looks costwise like the wrong direction for thin films.

Little work is being done on extending performance and capacity of external storage media (tapes or disks) by a large factor. 4500 bits per inch have been recorded on plated tapes without phase shift, and work on even higher density and on close head spacing in San Jose is appropriate, but head frequency may limit its application in the high-performance area.

Conclusions

1. We must recognize that IBM will have to build a 10 to 100 times Stretch machine eventually. There is a clear need in several Government areas, and there clearly is competitive pressure building up.

2. Work on high-speed technology should be encouraged, not diminished. This includes semiconductor circuits, cryogenics, high-speed memories, packaging, and external storage.

3. More concentrated effort is needed in the machine organization area to solve the problems introduced by the new technology and to understand the needs of the customers. This should include gaining extensive experience with actual applications of both Stretch and Harvest, if we are to make real progress beyond these systems.

4. This is the time to get a study contract for a machine organization around 1 nsec circuits and appropriate memory configurations. It is too soon to define and get committed to building an actual machine.

5. When the time comes we should avoid getting two development contracts for the same machine for different customers.

6. FSD Bethesda should be studying new application areas for large computers.

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Mr. R. L. Palmer
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