Notes taken at "Stretch School"

Orientation Course Mon. am. Feb 16, 1959

E. Cowen. Introduction

9000 total in Poughkeepsie
5500 Manufacturing.
3000 Engr. PD-Res.
503 educ - prod test - CE's etc.

M. Shaler:

unique approach - since 701, a cadre (12 regional people) preping specialists -

- announcement will not be Apr 1, "for some time"

consent decree

special systems — delays, cost

official position — we will discuss special systems with a customer — a serious discussion, present STRETCH plan. — can discuss LA STRETCH with

whether smtht, somthg LA STRETCH or some other limit been decided

Dr. D. Newton will be Mktig STRETCH man.

S. Dunwell:

- a really high powered computa
- a new technology to be used Throughout IBM
  7090 - 7070 mems, cards, etc.
- part of system running now
  - runs 256,000 opns cycle $\frac{1}{4}$ sec.
  auto error cor. now working for most part.

some things were done on interim basis — will be fixed on later passes,

~250K Transistors.

automatic error correction.

Pendery:

recall days of 701

Electrodata was hurting CPC — now Honeywell

people wanted drum machine. — Transacs are beating

→ stopped producing after 200th

entire year behind on 704.

only IBM could have done this job.

contract first, then figure out what to do, then figure mkt. & pricing afterward.. } STRETCH was unique

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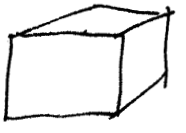
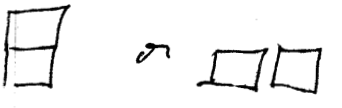
general design objectives ⟺ compromises

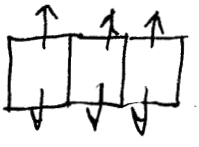
how did we get to where we are.

Sweeney: SMS Cube I/O equip.



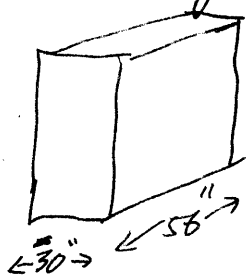
single or 2 high

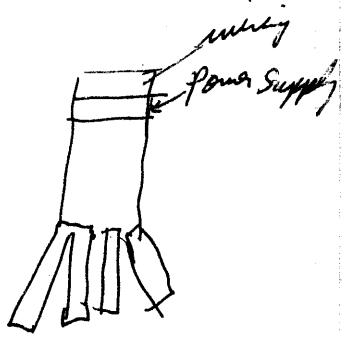




service from 2 sides

Rolldegon





more density needed
- double card

single slide

16K mem / frame, 30"×56"

Sweeney: Speed & Generality.

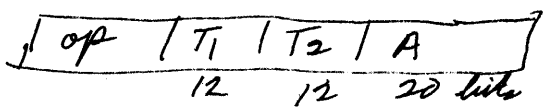
overlap: I/O & compute

universal accumulator. 10–15%

addressable registers,

index registers: 3 too few (inf. no. wanted)

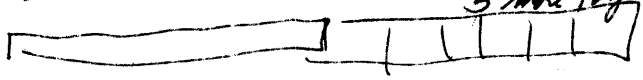
started with 4096



old formant

sum T_1 & T_2 also a limit.

give



next consider 2 address instr.

Then consider 32 bits. drop to 2^{16} wds, } for speed
2 instr/wd, 20% fewer instrs -}

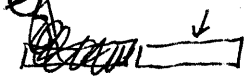
16 instr regs

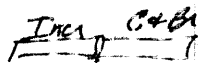
Index: generality would like.
Value / Incr / Compare / Tr. address / Refill

chose V C R

most common +1 -1

Adv + Count + Branch





pay for generality with time,

String of bits,
VFL
automatic monitoring e.g. 4 parity

Symmetry of sign control & (normalized)

Brooks: philosophy
goal 100 times & corresponding memory (10×?)
Some probs can't be attacked.
Cost per opn is issue.

General purpose :— computing & data processing & integrated or real time
(can be slow real time)

why not special purp. machines.
— non-specialized parts ∅ make up majority of cost.

STRETCH more new technology-generated than prob. generated

organization:
parallel op.
— lookahead on same prob. not 2 probs.

Instr. Set. 20% fewer

More efficient use of bits.
programming cost.
— cannot foresee what people will do.
systematization. (symetry
5 times as many things can be done than 709
with 40% fewer instrs.

Avoid specialization at expense of generality
(can't foresee all uses.) not a "super 704",
eg. editing are not so slick as 3 "converts" on 709 & many others
eg. interrupt not fixed to one type of fix-up.
eg. console — buttons.
but some cases have put in special ops. for common case
eg. sq. root; ∅ add, C & B

new techniques will replace some of old

-emphasize reliability & serviceability.

multiprogramming;

since cost for speed ↑

also hardware rent ↑ (cost per sec)

- I/O overlap
- interrupt
- multiprog. — can go to next task. & leave stopped prob

requires: (1) interrupt system
(2) address protection

flexibility

→ "power rather than protection." fundamental assumption

waiting now becomes man time not machine time.

-closer ties between man & machine — man looks at special case.

Mems 2^{14} wds 2^{20} bits

can get 16 mems.

2^{18} wds 2^{24} bits.

Disk --- will replace many of small tape jobs.

Noisy Mode

1. Raw speed
2. Quietness of attach - power

- too fast
- prog examples not enough
- manual
  - fit format

Comparisons vs other machines

instr. Times ← [illegible]

Speed of progs double + triple precision.