January 14, 1959

MEMO TO: Mr. D. W. Sweeney

SUBJECT: KMPD

SAC - SAGE

The first machine is required by SAC about April 1960.

SAC-SAGE is a synchronous machine with a basic cycle of 2.56 usec. and a timing pulse length of .160 usec. This cycle length permits complete overlapping of single-indexing with other functions. Double-indexing, however, requires 4 extra timing pulses (4 x .160 = 640 usec).

Fixed point times are given below.

Load, Store	5.12 usec
Add	5.12 usec.
Multiply	11.10 usec.
Branch	2.56 usec (whether taken or not).
Divide	(about the same as multiply).

Times given for the following fixed point program show that some overlap is possible. It is assumed that the branch instruction refers back to the load.

Load	2.56 usec
Multiply	8.64 usec
Add	2.56 usec
Store	5.12 usec
Branch	2.56 usec
	21.44 usec

This is about 15.8 times 704 speed on this loop.

It is too early to put much confidence in any floating point times quoted. Best current figures are —

Add	25-30 usec
Multiply	20-40 usec
Divide	40-80 usec

These rates applied to the above loop place SAC-SAGE at 4-1/2 to 6-1/2 times 704 speed on floating point.

Army Program

Many names have appeared in connection with this program. Among them are Mobydic, Basicpac, Logicpac, and Informer. They refer to portable, field computers. KMPD has contracted to build one each of two machines using pulse core logic. These machines were formerly called Management Central and Informer but now are called Data Coordinator - Retrieval. This dualized name reflects the construction principle that a large part of each is identical.

This identical part is called a Standard computer and is itself a progeny of another computer called the Base computer. The Base computer uses its main memory to simulate as many CPU registers as possible, and other steps are made to reduce hardware to a minimum. Thus, the Base computer weighs only 175 pounds and operates at around 20,000 instructions per second. (Main memory is box of core storage - 4096 words at 8 usec/word — that rests on top of the computer.)

The Standard computer is the Base computer plus an Accellerator. The Accellerator puts into hardware some of the registers simulated in Base. The Standard operates at about 40,000 operations per second and weighs about 275 pounds. A Super computer at 60,000 operations per second is formed by adding yet another Accellerator.

KMPD will add a disk unit to a Standard computer to form a Data Retrieval system and will add certain other special hardware to a Standard computer to form a Data Coordinator system. Philco has contracted to build a Base and a Standard using transistor logic. In the contest, Philco will probably have trouble meeting the weight constraints. To the victor is a fat production contract.

The modularization and miniturization goals in this program should be of great interest to Product Planning. I would like to renew my suggestion to Paul Seever that a speaker from KMPD (perhaps Ralph Marden) be invited to address one of our future department meetings.

Jack C. Gibson

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JCG:jcj

cc: Mr. D. W. Pendery
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