Series of Discussions with Engineers concerning changes possible in STRETCH

<u>7000-X meeting</u> :

Ulfsparr, Blaauw, Kolsky

<u>Dec 17, 58</u>

<u>Present status</u> ?

2 Ref no. or 2 Jks.

Sigma Bus: 1 frame handles 6 memo (not sequent.)

Sigma: I Box all fetches (3 regs.)
LA all stores

1 chan. <u>addresses</u> are diff

300 Trs. per line?

no box

B. Exch. ~(17K Trs.) — requires 4.5 us service.
H.S. Exch. ←
Computer.

<u>Tr Savings?</u>

no registers in bus now.

~ 3400. Transistors in Sigma Bus. (14K Harvest bus)

Sumin was cut to 2500 Trs. — using exchange Trs.

~ <u>3000</u> Transistor — guess at 7000-X.
not incl checker

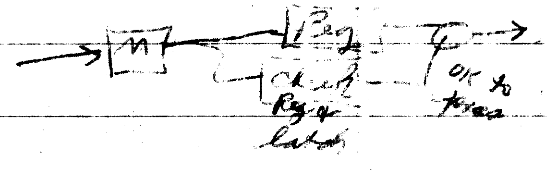
~2000 Trs. for checker (with own registers) — could go to 1500 with other reg

<u>Time Savings</u> ? (gates are expensive)

yes 1 Transfer cycle to get in 0.3 us
1 " to get out 0.5 us

~~would save ~0.2 us on each fetch.~~

→ might be able to check in parallel & not add 0.4 extra. (ref. fig. 2)



If there were 2 boxes interleaving?

— add back busy triggers.

every channel has devices

(no channels)×(no mems.)

[illegible] (3 × 2) = 6 × 20 = 120

instead (5 × 6) = 30 [illegible] = 600

Time savings about the same

Design Effort:

small, especially now we have circuits,

— do have to "balance", etc.

~~same ideas would be used.~~

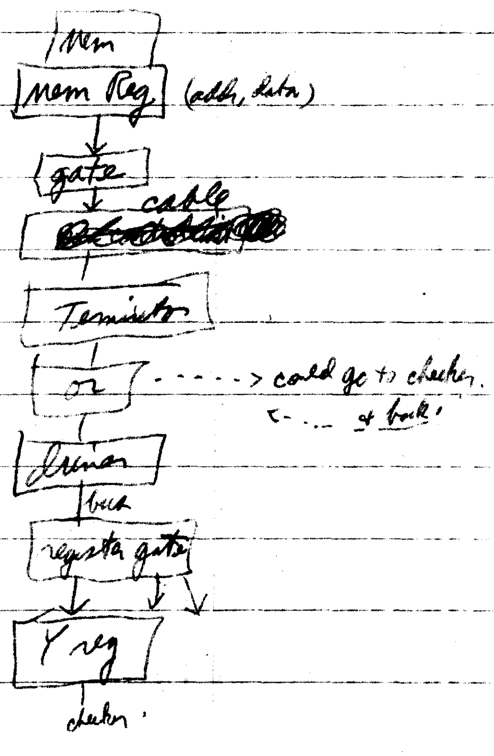
— equipment for 2 mem speeds — also considerable

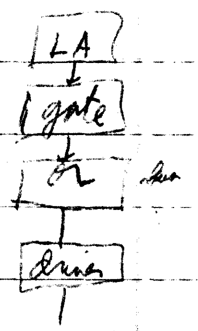
checker { not separate for fetches + stores, ...
{ also by making slower — don't have to pyramid, made cheaper

---

present trouble — too many gates off same register

— all registers would be put on same bus checker?





7000-X Meeting

Dec 17, '58

Hipp: (Serial Arith Unit.)
Lou King, Kalisky, Bleauw

HS. 12,000 Transistors excl. controls.

Mpy: add & shift.

question of combining Δ,(f) and A-B? — not good idea, already too many gates etc on AB.

— cutting out cross-wd boundary work wouldn't be big saving.
— counters on connects — cost a lot.

- VFL is now 1½ frames.
  for data flow, arith unit, controls (regs etc)
- checker ½ frame

"guestimates" ~32K, may be lower.

· Fl Point 2 frames — ~33K trs.

Speed: 0.5 μs/byte — "tight" — may be influenced below this — distances, etc.

[Regs are detailed, dataflow being detailed, controls are worked out not being detailed yet

7000-X:

Floating Point Arith Unit

McSorley:

Dec 17, '58

H.-S. Mpy | remove + do in adder – different decoder + control. Save about 1/4 of Trs.

Mpy | would be ~ 9 or 10 μsec. (average due to no of 1's + 0's)

adds when there are changes from 0's to 1's.

Div could stay as is or be same as Mpy.

Entire F.P. unit at present

question of restricting no. of shifts? – not a big saving, but some.

2 Transistors per bit. 200 Transistors to remove 1 shift

– at present have

shifts of left 5, left 6, left 4, left 3, L2, L1, 0, R1, R2, R3, R4, R8

R8 used for VFL

~ 2000 Trs.

question: reducing adder to 48 bits

– would cost time in double precision (can cost as many as 4 passes thru adder on end-around-carry.)

– mpy wouldn't be changed too much

– some added control complexity.

(would have to redefine single precision.)

0.6 μs per pass.

– divide would be slowed down – or have ~~another place to store. – more compl. controls~~

26K Trs. without adder ~6K (300 cards more) + checker ~3K

close to 540K at end. ~38K

not sep. frames

reg shifts 1 slide

adder "

mpy "

controls misc "

— register-shifter could be cut in half — but very messy on normalization.

question: using AB as working reg
- slower — longer connections.
- can't modify registers in some cases while checking is being done.
- cum. mpy would be problem.

HS Mpy: 38K transistors → 28K

Addr in half: (40 bits ~20 ~800 Trs) 28K → 26K

Engineering effort? depends on amt. of change
- just cutting out isn't bad — but improvement might not be enough, — so that redesign would be in order.
- with same general principles would still save a lot of Time — to use std cards + circuits.

7000-X:

Kallaran: I-Box design Dec 17, 58

Buffer Reg.

probs of "no-oping" – can't store old information
would have to count

– one mem. – simplifies

most of I-Box gain in extra Y reg & in controls. – Extra sequencers – guessing on decode instead of taking extra cycle.

VFL requires versatility, Fl Pt requires speed ← could simplify here

4 sequencers here — no change — 4 sequencers here

need two Y's on Transmitt cross-wd buses.

having exchange mem. – would make little change in I box,
X mem, ~1000 Trs & cores.

~30 K transistors — registers all different – some wastage

now ~35K Trs. — controls were underestimated ~5K

16 panels. not incl interrupt

one mem at Time

– hurts bad timeconsole.

– would try for synchronous to mem – very straightforward. – exchange

– wouldn't make paths as tight – "fat" and "create" now to leave redesign? – data flow would be similar – would not be big change.

common checker ? — would be more efficient to keep.
— still have residue control out 3.

Interleaving 2 mems? - I box does not pay attention to this mem- (half mic. mem)
— if one can't depend on mod coming back — there is no saving if one has delay. — question of exchange —

— fetching from single location.
— not separate adder for I. C.
— index adder itself could be some simpler. — still parallel serial carry in header to check?

Tr. count? hard to guess. reduction. still ~ 30K Tr. if we use present IBx
22K but flow same

redesign: — redesign would be much less than starting from scratch.

What versatility cost most?

— programmed indexing
— all full word instrs.
— crossword boundaries
— interrupt system
— different length fields
— causes lot of testing & loading L.A. etc.

peculiar → — geometric load 750 Trs.
— Transmit - Swap (all in controls)

peculiar → — Rename hard to no-op.
— Execute & Execute Indirect
protective devices
boundary compare (hard to control)

- can cut Z registers in half. (has sequencers, and tag registers duplicated too,) but would hurt performance — even old Basic would have it

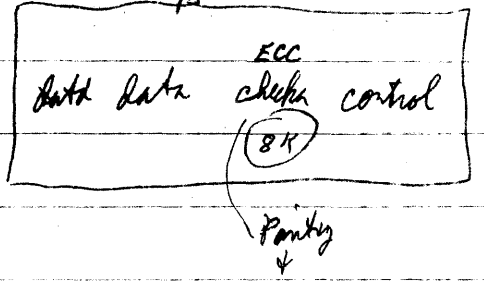
Old Basic had only one V reg: (was in + out)

Probably can't charge I Box much + keeps 15-20 x performance?

Registers are not dynamic if they have simple gating.

Dirac: ~~Look Ahead~~.

I Box



present Look Ahead

8K per gate Total ~22K

remove 3 levels: 9850 = ~12K

a one level LA