Meeting Concerning Simplifying Sigma — Mon, June 9 58

E Block
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* Part time

Present Status:

FLPt	28%
VFLauth	18%
Instr Ext	18%
Look Ahead	16%
Checking + Maint	20%

140,000. Trs
not incl, Mem Bus,
want to get down to ~ 100K.

Keep perf. up – reduce cost.

I Box – Look Ahead area:

propose drop to 3 levels. (5000 trs.) about square law

1. Contractual Speeds — imp. but a satisfactory 1 to IBM machine (commercial)
2. Comercial Program – does depend on Ix count.

4th level of look-ahead:

1. does qualify under square law
2. does get better for high perf. buses, etc.

Simulate → question: shorten read out time vs. no. levels of L.A.

- Interrupts, don't update indicators — ← programmer can handle
- don't compare fetches vs LA stores — ← Suggest compare on low order 2 bits only
- I Box fetches operands for LA

Simulate: Interlock so only one ref. can take place at once
—may already be?

Extra Buffer in I Box ⇒ very important to have one.

} Same principle as 1st level of look-ahead.

Eliminate Wd. Boundaries cross over for instrs.

| half, half | half, nop | full | ~~[illegible]~~

↑ would have to be put in

simplify I box — may be faster — ?

divide → leave in

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algebraic sign in Index Arith.
(one way only.) —

adder would go from 1.0 to 0.8 by removing these gates.

true or complement form in X Regs only?
— principles are important here —

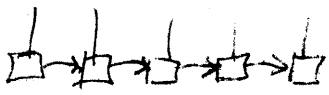
ignore low?

Elim. Progressive Indexing;
— take "on faith" here.

Address Comparisons
~~Add~~ - vital to 2000 A.

quarter of size of locking —

equal.
unequal.



performance question —
comparison is overlapped in time now.

block to 8000 wds? 1000 trs.

what about 256. wds? low order 8 bits

⇒ Check into Supervisor Prog. etc. to see effect same 600 trs.

(e) Elapsed Time Clock:

2^{18} millisec $\tilde{=}$ 8 min

(g) Elim. Dec. Arith. mpy-div only. ? or add also.

(1) all: ~~3000.~~ Tra. (also get timing with Loop. from .450 to .900 μsec 2 logical levels.

(2) mpy-div only: 2700. Tra, (no time gain)

compatibility — Sigma bre. to subroutine. ?

or nothing. ×

20 bits { Mpy 13 / Div 18 add 2.2 μs ~~20~~ 20 bits

5 digits { Mpy 65 μs / Div 94 μs · 3.5 μs 5 digits

→ looking into this — from point of view of conversions, on commercial.

(f) ~~Loop~~ "Costly ops:"

(will go over this to see LA running) →	Execute & Indir. Execute	500.	Transistors — (very hard on look-ahead — must keep.
(discuss later) —	Rename	200.	— will simplify (many faults)
(1.5 μs per index added +3 μs) →	Load ~~Indirect~~ Indirect	300.	— must keep in.
	Geom. Load.	500.	— keep in (Talk to Los Alamos)
	Store address.	100.	— very important
		1600.	

(h) left zeros & all ones ctrs 2,500. trs.

very fundamental new concept.

Summary:

?	1. Checking (not discussed)	6000.	— later discussion.
?	2. 4th level of LA.	5000.	will look at with S/M
½OK	3. {I-fetch LA	600.	" " " (if necess)
OK	4. Lo order bits of LA comp.	500.	agreed to
?	5. address compare	600.	look into
?	6. Rec, Mpy Div	2700.	look into.
?	7. Execute - rename	?	
		15,400.	