

Design Specifications for a High Speed Scientific Computer

A. Purpose

1. The STRETCH scientific computer should attempt to provide our customers with the latest advances in computer engineering technology and construction. This design should provide extremely reliable components and circuits utilizing transistor technology to provide a large scale Data Processing System capable of extensive periods of unattended operation. The arithmetic speeds and data handling capacities should be aimed at solving problems already in existence but not solvable on existing Data Processing Systems. Performance at 100x 709 computing speeds should be the goal.

B. Market

1. Immediate applications of this system are found in AEC installations, where large scale reactor calculations involving many millions of data items are known, but processing on existing Data Processing Systems requires excessive periods of time.

With advanced programming techniques in automatic coding and auto-monitoring, this system should have value to installations having medium size problems in quantity.

2. This system should provide a temporary upper bound on the product line. With one or two additional computers filling the performance and rental gap between the 709 and this machine, a complete range of computing versatility would be available to our customers.
3. The rental objective for a standard system should lie in the range of \$150,000 - \$200,000 per month. Under extreme conditions a maximum of \$250,000 should be considered.
4. Five year sales figures are not available at this time.

C. Fundamental Characteristics

1. The STRETCH high speed scientific or technical computer should consist of the following major components:

1.1 Memory: This component should have three subdivisions.

1.1.1 Main Memory - consisting of units of 16,384 words of core storage having a full read-write cycle of 2.0 us.

1.1.2 Fast Memory - consisting of units of 1,024 words of core storage having a full read-write cycle of 0.5 us.

1.1.3 Ultra Fast Memory - consisting of 16-18 words of register storage or a (non-destructive core matrix with a cycle time of 0.2 us.) ?

When more than one unit of memory is present the units should be multiplexed so that consecutive words appear in adjacent units. Units should be added in groups that yield binary powers i. e., 1, 2, 4, 8, units should be the main memory configurations. The faster units should occupy the lowest addresses. Fast memory should be available up to 4096 words.

1.2 Control Arithmetic Unit Decoder: This component should be able to obtain instructions requiring processing in the Main Arithmetic Unit. It should perform any required indexing and obtain, if possible, any data required by this instruction. The indexed instruction and pre-accessed data should be "stacked" in a buffer-system or "look-ahead" to await execution. At least four levels of such buffer storage should be provided between the indexing process and the final execution stage.

1.3 Main Arithmetic Unit: This unit should be able to operate in the fixed point or floating point mode. In the floating point mode provision should exist for operating with "normalized" or "unnormalized" numbers. The word length used as standard should consist of 64 binary

not mode!

bits and sign for fixed point numbers. For floating point numbers there should be a 12 bit signed exponent and a 48 bit signed mantissa. This unit should be capable of repeating a given operation, should the checking circuits indicate an erroneous computation. This implies retention of the operands throughout the computation.

- 1.4 Input-Output Computer: This unit should handle all operations not directly concerned with the Main Arithmetic Unit. With respect to the Main Arithmetic Unit, its action should be essentially independent. For scientific computer uses, this Input-Output Computer should be able to process all I/O instructions and perform the necessary editing required to make data available to the Main Arithmetic Unit. Instructions dealing with this unit of the system should be indicated by means of format control or special tags. It should be kept fully in mind that this computer can act independently or concurrently with the Main Arithmetic Unit.
- 1.5 Exchange: This unit should fulfill the following functions:
 - 1.5.1 Interconnect specific I/O units to available channels.
 - 1.5.2 For input - assemble the bits of the characters into full computer words and initiate action to place completed words in specific locations in the memory.
 - 1.5.3 For output - obtain specific words from memory and disassemble such words into characters for transmission to output devices.
 - 1.5.4 For control - accept information from the I/O computer and use this information to control the actions of I/O units connected to the exchange.
 - 1.5.5 For checking - allow suitable error correction and detection devices to monitor the flow of information.

- 1.5.6 Provide for automatic assignment of I/O units to available channels.

2. Input-Output Equipment

Considering the extremely wide range of I/O devices available for this system it is possible that more than one type of Exchange might be required. The possible major types of I/O that should be considered are:

2.1 High Speed

- 2.1.1 Disk Storage - units of 1,048,576 word capacity leaving continuous 15,000,000 bits per record information transfer for each unit.
- 2.1.2 Magnetic Tape - if available tape units of 100x 727 tape should be connectable to the exchange which handles the Disk Storage.

2.2 Medium Speed

- 2.2.1 Magnetic Tape - Tape units characterized as 60K tapes should be the main tapes for this system. They should move at the rate of 112.5" per second and have a bit density of 533 bits per inch. In addition tape units characterized as 15K tapes should be permissible. These tapes are specified as having a speed of 75" per second with a bit density of 200 bits per inch.
- 2.2.2 Electronic Printer-Plotter - Permitting page printing or plotting with recording on microfilm with an associated visual display. The printing rate should approximate 16,500 characters per second.
- 2.2.3 High-speed direct printer - Operating at 1000 lines per minute with 120 characters per line and automatic checking.

2. 2. 4 High-speed card reader - Operating at 500 cards per minute. If available, 1000 card per minute card reader should be utilized.

2. 2. 5 Card Punch - Operating at 250 cards per minute if available.

2. 3 Low-Speed

2. 3. 1 Manual Keyboard and Typewriter - used to interrogate the system. For operator control and "debugging" from remote stations these units should be most important.

2. 3. 2 Real-time devices - direct telephone or transceiver connections should prove increasingly valuable in data reduction and data collection problems. Two way circuits should enable this computer to serve as a real-time guidance system or as a control monitor for certain types of studies.

2. 2. 3 Visual displays to serve as observable output where the speed of the Electronic Printer-Plotter is excessive.

3. Checking

The checking system should be able to detect and correct single errors and detect most multiple errors. Whenever an error is detected and corrected, the machine should record the circumstances of the error. This information will then be available to the customer engineer for later analysis, location, and correction of the faulty component.

4. Performance

Every attempt should be made to meet the following Main Arithmetic Unit speeds:

4. 1 Add and Subtract	0. 2 us - fixed point
	0. 6 us - floating point

4.2 Multiply 1.2 us - fixed or floating point
average

4.3 Divide 1.8 us - fixed or floating point
average

5. Instruction Set

Analysis of present programming techniques has indicated a need for generalizing machine orders dealing with logical connectives, indexing, improved floating point accuracy and significance testing. Improved techniques for indirect addressing and the necessity for obtaining with the operation, data values to be used immediately are also indicated as very desirable.

While construction of the instruction set should include consideration of ease of programming for those who will code using standard technique it should be realized that the bulk of programming for this system will probably utilize techniques of automatic programming. Further, unattended machine operation implies the ability to execute efficiently automonitoring or supervisory programs by the system itself. This feature is particularly important where real-time applications are likely to be encountered. It should be feasible for this system to process problems subject to intermittent interruption from input-output devices with particular emphasis on data-reduction problems.

Edward W. Coffin

E. W. Coffin
January 21, 1958

EWC/jcv
DISTRIBUTION:

Mr. E. F. Codd
Mr. J. C. Gibson
Mr. H. G. Jones
Mr. H. G. Kolsky ←
Miss B. McDonough
Mr. B. Moncreiff
Mr. D. W. Pendery
Mr. D. W. Sweeney