March 25, 1957

HARVEST REPORT #13

Subject: Checking, Byte Selection, and Indexing in the Continuous Stream Register

References:
1. Machine Specification Report #2, "Continuous Stream Register", S. W. Dunwell, 9/6/56
2. Harvest Report #14, "Control System for a Simple Continuous Stream Register", J. H. Pomerene et al., 2/1/57

The major features and philosophy of the CSR are given in the above references. The present report consists of three largely self-explanatory figures together with some pertinent comments.

Figure 1 shows an overall view of the CSR with its indexing equipment. The particular indexing scheme is that of P. S. Herwitz as described in Harvest Internal Note #9, 3/14/57. Given a present address which is controlling both the present word content and present byte selection of the CSR, the next address can come from any one of 4 sources. The three sources on the right have to do with the streaming mode of the CSR. Full hardware is shown for the second index level because in many typical applications the first level can be quite short (say $N_1 = 3$) and excessive time would be consumed in repeatedly obtaining and testing the second level index word. The leftmost source handles regular, as opposed to streaming, operations and is given its own hardware so that regular instructions can be performed in the midst of streaming and without disturbing the stream setup. Since regular instructions as presently envisioned specify a start point in memory and a field length (in bits) of up to one word, the mechanism is arranged to process the field in 8 bit chunks.

Figures 2 and 3 show a byte selection mechanism which incorporates checking by means of simple parity. The same scheme could be elaborated to include higher levels of parity for error correction if necessary. The selection is done in two levels to affect a considerable saving in equipment. The one level scheme described in reference 2 required 1024 switching intersections without checking, while the

present scheme requires only 304 intersections without checking or 408 intersections with checking.

Figure 2 shows the parity generation and the first level selection matrix. Most of the parity generating equipment is that which would be needed anyway to check words read into the CSR from memory. The 4 high order bits of the byte address (a double length CSR is assumed) control the first level selection.

Figure 3 shows the second level selection matrix (shown only as a box in figure 2). The 3 low order bits of the byte address cause one of the diagonal selection lines to be energized thus selecting one of a set of eight 8 bit bytes from the 16 data bit outputs of the first level. The 8 remaining bits plus the parity bit are also selected into a 9 bit "residue" byte. The overall parity of the 17 bits can be checked from the parities of the selected and residue bytes together. The parity of the selected byte alone is available at the output of the CSR.

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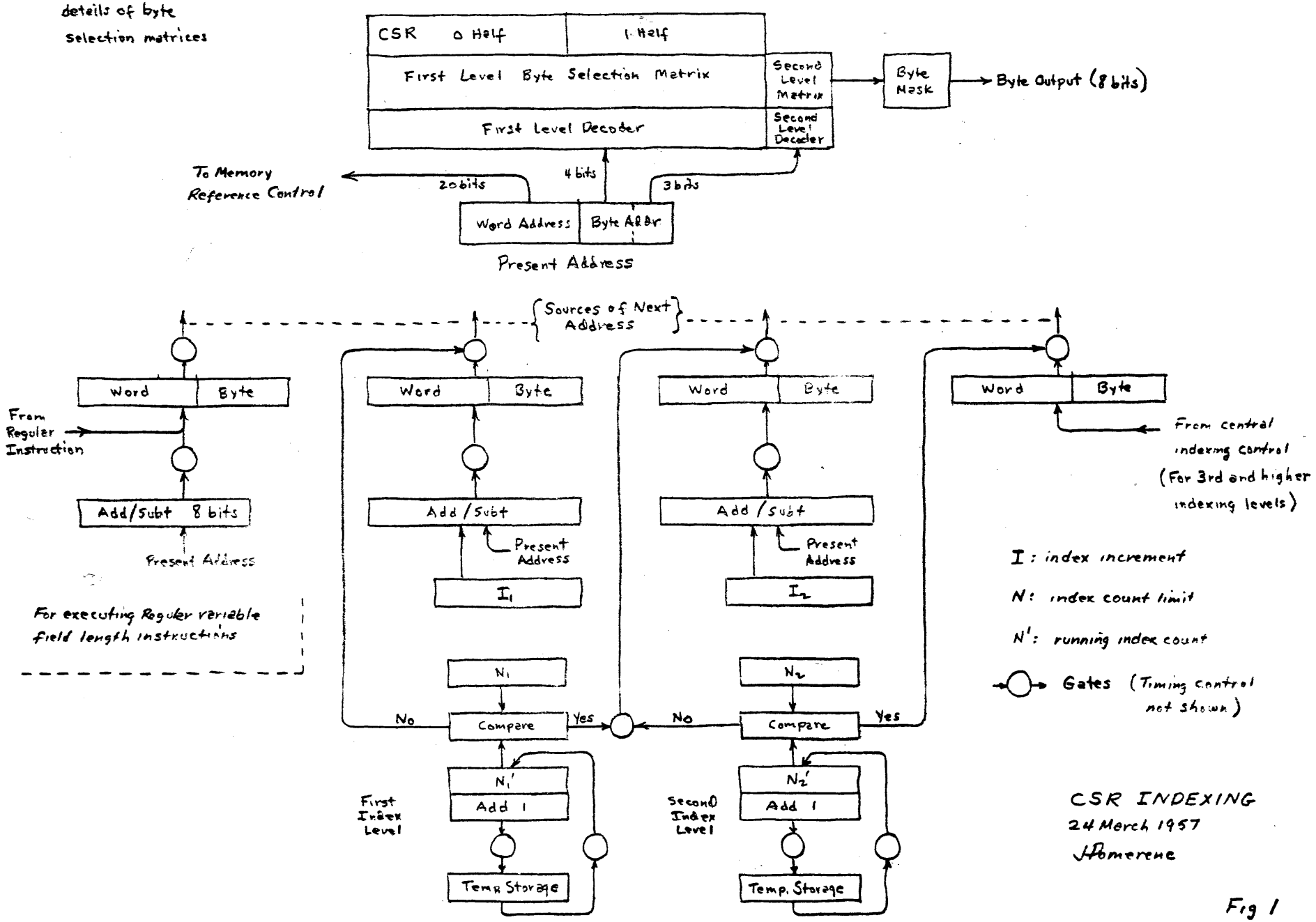
See other dwgs for details of byte selection matrices



CSR INDEXING
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Fig 1

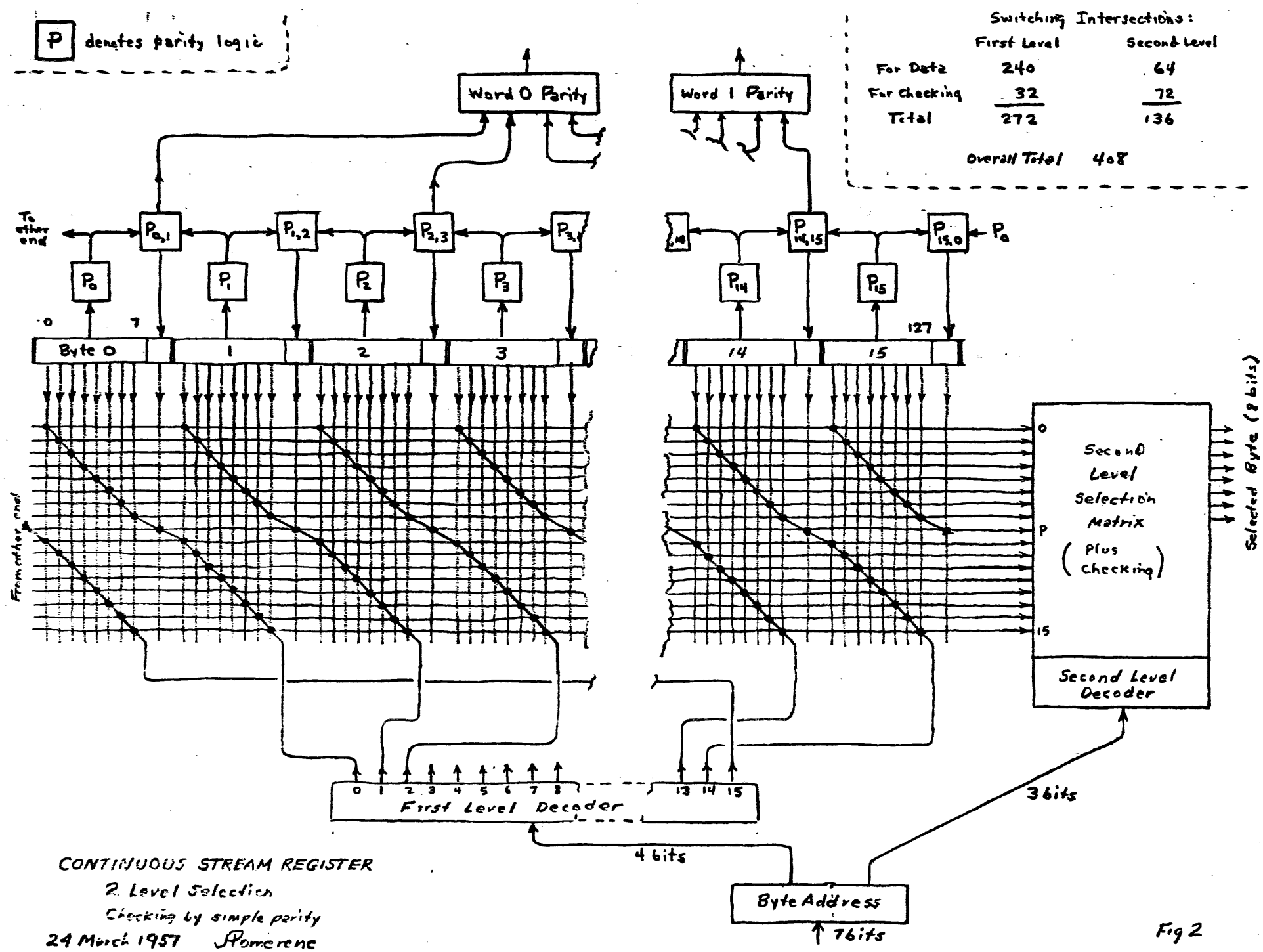
P denotes parity logic
Switching Intersections:
First Level
Second Level
For Data 240 64
For Checking 32 72
Total 272 136
Overall Total 408
Word 0 Parity
Word 1 Parity
To other end
From other end
Byte 0
1
2
3
14
15
127
Second Level Selection Matrix (Plus Checking)
Second Level Decoder
Selected Byte (9 bits)
First Level Decoder
4 bits
3 bits
Byte Address
7 bits
CONTINUOUS STREAM REGISTER
2 Level Selection
Checking by simple parity
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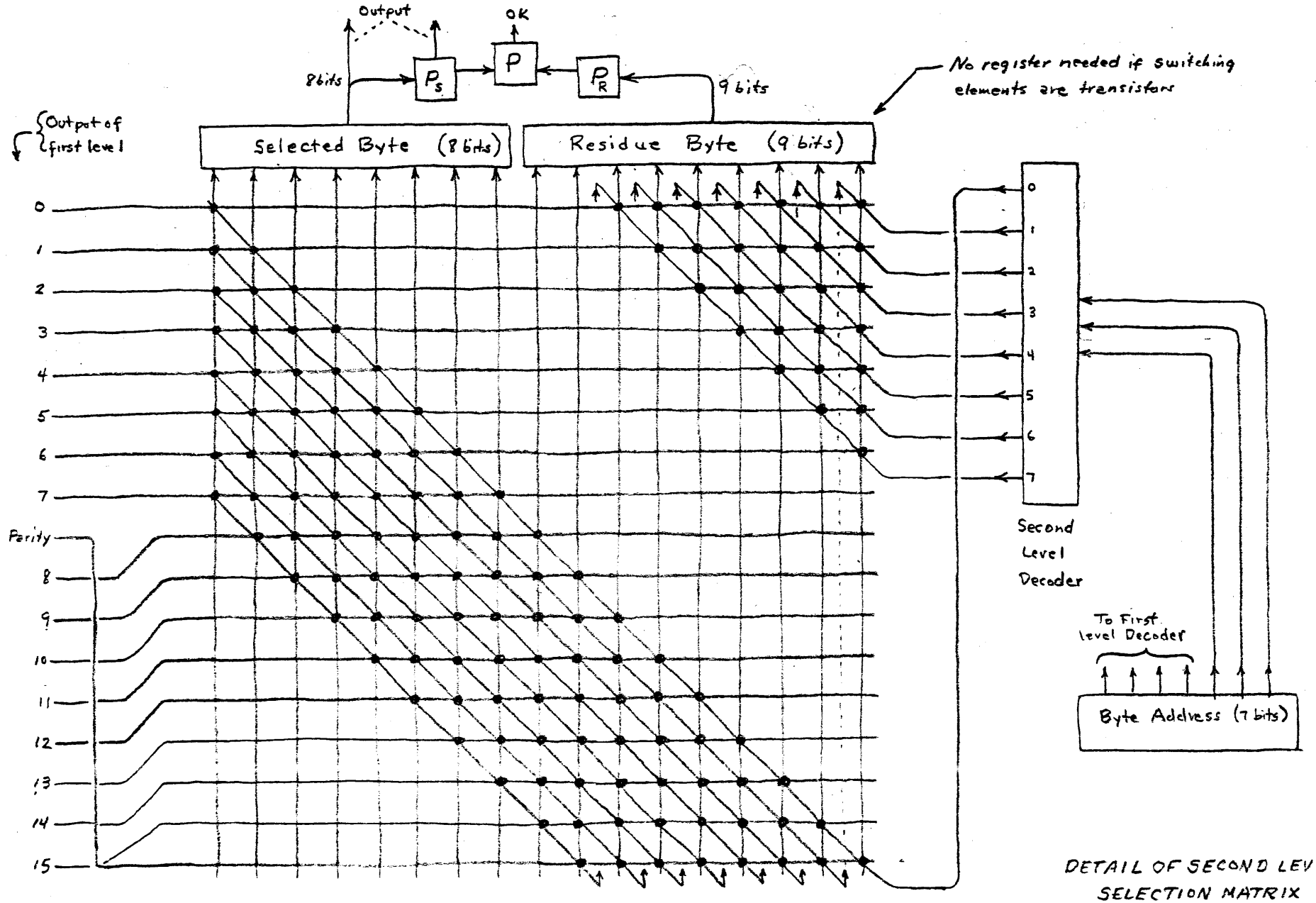
Fig 2



Switching Intersections:

64	for data
72	for checking
136	Total

Note: [P] denotes parity logic

DETAIL OF SECOND LEVEL SELECTION MATRIX

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Fig 3