Major Units in the 7030

1. Main memory (sometimes called external memory)

6 boxes of 16K extended word each for the Los Alamos configuration. Each extended word contain 64 information bits plus 8 error-check bits

Controlled by the memory bus control unit (MBCU) which aside from initiating all accesses to main memory, also monitors the submitted addresses for "address invalid" condition. The MBCU has direct contact with the following units: memory boxes, Exchange, Disk Exchange, Lookahead and I-box.

2. Instruction unit (I box)

Contains the instruction counter (IC), the 16 index registers ($0-$15), the Time clock ($TC) and Interval timer ($IT), the "originals" of the index condition indicators ($XF, $XVLZ, $XVZ, $XLGZ, $XCZ, $XL, $XE, $XH), and many registers, circuits needed for efficient decoding and execution of instructions.

Generates all instruction fetch requests on the basis of IC contents. Develops effective addresses by adding the pertinent index value to the numerical address.

Generates E-box operand requests for Lookahead.

Partially decodes E-box instructions and converts the latter into information suitable for Lookahead processing. This information is then loaded into Lookahead.

Decodes and executes all index arithmetic instructions as well as the following: Z, R, RCZ, EX, EXIC, T; SWAP, except that stores are performed with the help of Lookahead. If non-I-box opnds are required they will be fetch from the MBCU or the Lookahead.

Decodes and executes the following "unconditional" branch instructions: B, BE, BD, BR, BEW, CB, CBR and Bind for the index condition indicators. The complete execution of BB and Bind for non-index conditions require the assistance of the Lookahead and the E-box.

Submits indicator conditions for the following indictors to LA for updating of the indicator register:

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$IF, $OP, $AD (from MBCU), $DS, $DF, $IF + index indicators.
These indicators plus a "conditional machine check" may lead to interruption during the updating. Other I-box generated indicators are gated directly to the indicator register.

Updates $TC and $IT every 1/1024 sec.

3. Lookahead (LA)

Contains 4 buffer levels, an address register (LAAR) and five counters IAUC (I-box), ØCC (operand check), TBC (transfer bus into E-box), ABC (arithmetic bus and interruption system) and SCC (store check).

When IAUC refers to a level, that level may accept I-box loading, although the required operand may come later from MBCU. ~~or may~~

During Øcc time the operand from MBCU may be checked for error.

During TBC time the level may be shipped into E-box.

During ABC time the interruption system is updated, and signal is given to E-box for execution of instruction just loaded.

During SCC time the store operand (if any) is checked and sent to MBCU on the bases of the contents of LAAR.

Provides interlocks, plus close contact with the interruption system to ensure smooth, ~~automatic~~ autonomous and error-free operations of the various units in the computer.

4. Interupt system

Contains the indicator register ($IND), the mask register ($MASK), also $CA and $CPU. Has direct connections with I-box, LA, E-box and the exchange units to receive updated indicator information.

Interruption occurs if

a. System is enabled

b. a masked indicator bit is a 1.

Interruption sequence.

a. the left-most masked indicator bit position (say O.K) is noted.

b. I-box is house-cleaned except the ~~[illegible]~~ index storage

c. LA house-cleaning is performed. Recovery information is shipped back to I-box: This include all index register recovery information

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and the "interrupted" IC value.

d. Contents of $IA is fetched and added to K.0

e. Instruction beginning at the address C($IA)+K.0 is fetched from MBCU without disturbing $IF indicator.

f. The "free" instruction is performed with all masked interruption conditions enforced. This intruction may or may not alter IC in I-box.

g. I-box fetches new instructions on the basis of IC. Resumption of normal operations.

5. E-box (Arithmetic unit)

Contains a parallel arithmetic unit (PAU) for floating-point fraction operations as well as all executed *, /, *+, and binary-decimal conversions.

Contains a serial arithmetic unit (SAU) for variable field length operations (except *, /, *+ and conversions), also for floating point exponent arithmetic.

Receives instructions and operands from LA for decoding and execution.

Submits store operands to LA, arithmetic indicator bits to the interruption system.

Contains the following registers:

Accumulator ($L, $R) and sign byte register ($SB).

Buffer registers C, D.

PAU buffer register F.

Left zero counter ($LZC) and all ones counter ($AØC).

6. Exchange

Contains 32 (32-63) channels for simultaneous I/Ø processing. Through adaptors each channel can be connected to 8 tape units or with one non-tape I/Ø unit. Each channel is represented by one control word and two data words in the exchange memory. The channels communicate with the exchange memory thru a "multiplexer".

Contains a main memory address register (MMAR) and a buffer register to communicate with the MBCU

Contains an interruption address register (IAR) which indicates the channel address for the channel which has created an interrupt condition. Contains Triggers To indicate the reason for interrupt: EØP, UK, EK, EE and CS. These triggers

and IAR contents are not until the interruption system accepts the conditions. When IAR is busy ("interrupt wait" trigger on) other channels cannot use it to cause other interrupts.

Accepts I/O instructions from LA (2 levels per instruction).

Fetches and stores control words and data words directly from MBCH subject to $AD restrictions, but not $DF and $DS as these are performed by the I-Box

Communicates with I/O units (thru adapters and multiplexer) in 8-bit bytes

Has its own clocking circuit (0.1 μs/cycles) and ECC check bit generator-comparer. Maximum word rate is 1 extended word / 10 μs for the entire exchange.

7. Disk exchange

Contains 32 channels (0-31) only one of which can be in operation at any given time Contains enough memory for 1 control word and 1 data word. Each channel can be attached to one disk unit.

Disk word rate is 1 extended word / 8 μs. No direct chaining of I/O control words is permitted Otherwise the disk exchange functions in much the same way as the exchange.