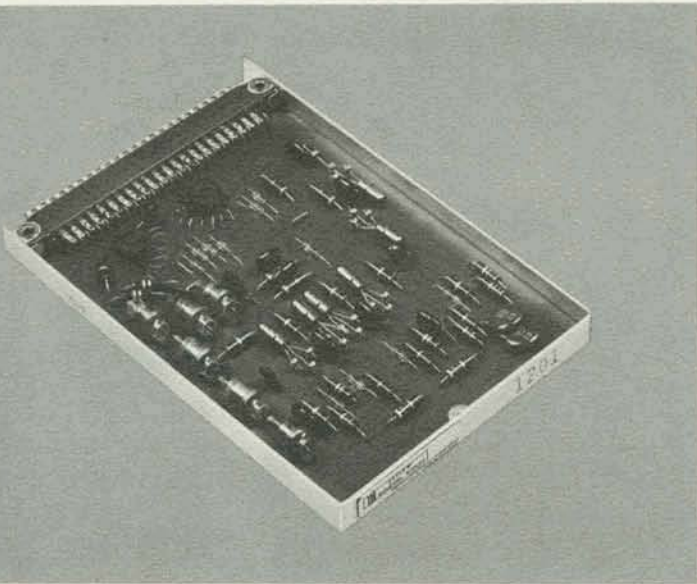


PROGRAMMED DATA PROCESSOR

DEC

programmed data processor



Flip-Flop Type 1201, one of the standard DEC System Building Blocks used in PDP-1.

The Programmed Data Processor -1 (PDP-1) is a fast, general purpose digital computer. It is a single address, single instruction stored program machine operating in parallel on eighteen bit one's complement binary numbers. Two special arithmetic instructions, multiply step and divide step, are the iteration steps for multiply and divide. Multiply takes approx. 350 microseconds and divide about 600.

The Programmed Data Processor is assembled with Digital Equipment Corporation's reliable and well proven System Building Blocks. The PDP-1 is fast and competent yet relatively inexpensive because of the unique combination of speed and versatility of these Building Blocks.

input-output

STANDARD EQUIPMENT

Flexowriter for reader, punch and input-output typewriter.

or

Separate input-output typewriter, punch and photoelectric tape reader.

OPTIONAL EQUIPMENT

Cathode-Ray-tube display
Magnetic tape
Real time clock
Analog equipment
Special equipment as required

PDP-1 with 1024 words of memory and standard input-output: Approx. \$85,000

PDP-1 with 4096 words of memory and standard input-output: Approx. \$110,000

PDP-3 — a 36-bit, very high-speed machine featuring 25 microsecond multiplication:
Approx. \$220,000

The input-output system of PDP-1 is simple and flexible. If simultaneous operation of several devices is required, a special multiple sequence automatic interrupt system is available.

- 100,000 to 200,000 instructions per second
- Random Access Core Memory – 5 usec cycle
- Indirect Addressing – multiple step
- 12 shift instruction variations
- 10 conditional instructions
- Flexible Input-output
- All solid-state logic circuits

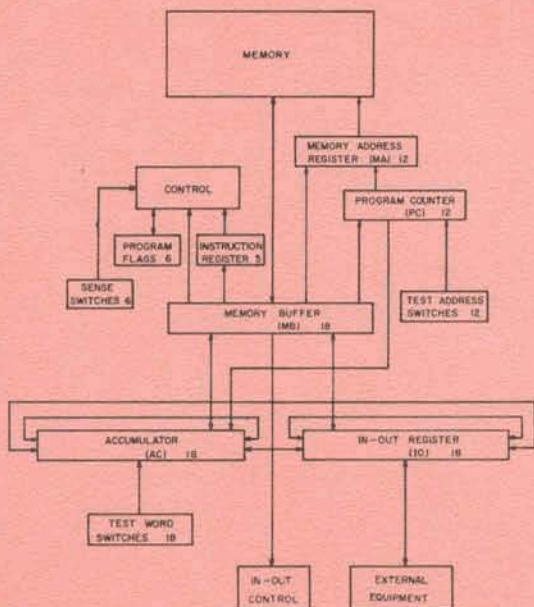
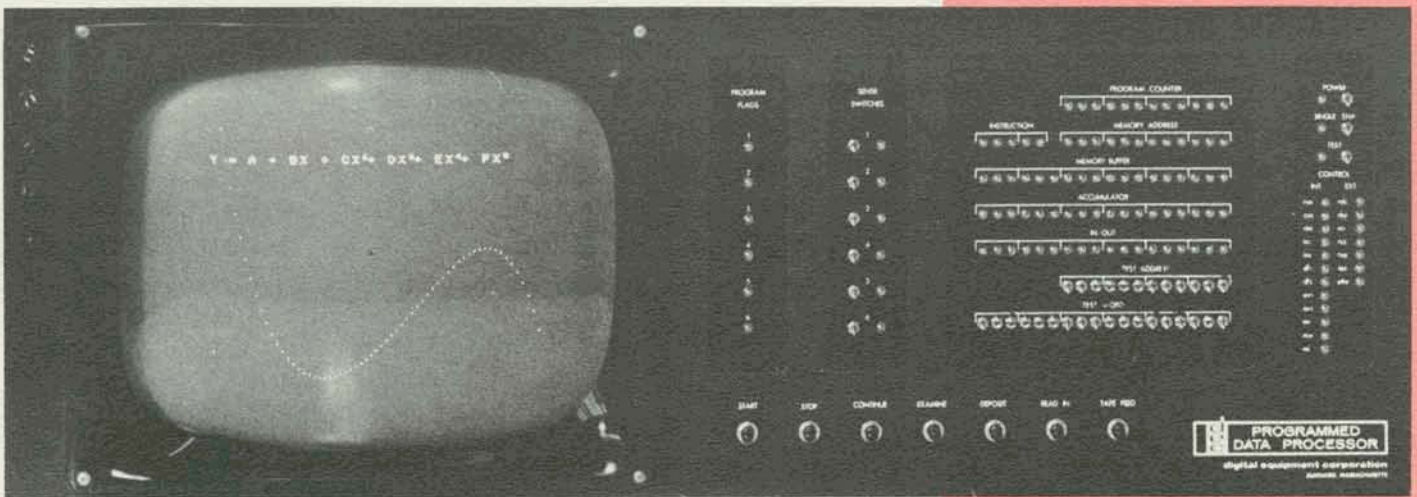


FIGURE 1
PDP-1 SYSTEM BLOCK DIAGRAM

INSTRUCTIONS

All memory reference instructions (add, dac, jmp, etc.) may use an indirect address. The address parts of iot, opr, shift, and skp are used to specify variations of the instruction.



FIGURE 2
PDP-1 INSTRUCTION FORMAT

PDP-1 INSTRUCTION LIST

BASIC INSTRUCTIONS

Instruction	Code	Explanation	Oper. Time (usec.)
add Y	40	Add C(Y) to C(AC)	10
and Y	02	Logical AND bits of C(Y) with C(AC)	10
dac Y	20	Deposit (store) C(AC) in Y	10
dap Y	26	Deposit address part of C(AC) in Y	10
dio Y	32	Deposit In-Out Reg. in AC	10
dip Y	30	Deposit instruction part of AC in Y	10
dis Y	56	Divide step (use in divide subroutine)	10
idx Y	44	Index (add one to)C(Y). Leave in Y & AC	10
ior Y	04	Inclusive or bits of C(Y) and C(AC)	10
iot	72	See In-Out Transfer group	—
isp Y	46	Index and skip if result is positive	10
jmp Y	60	Take next instruction from Y	5
jsp Y	62	Jump to Y and save Program counter in AC	5
lac Y	20	Load (clear and add) the AC with C(Y)	10
law Y	70	Load the AC with the number Y	5
law -Y	71	Load the AC with the number -Y	5
lio Y	22	Load the IO with C(Y)	10
mus Y	54	Multiply step (use in multiply subroutine)	10
opr	76	See operate group	5
sad Y	50	Skip next instruction if C(AC) differs from C(Y). C(AC) and C(Y) left unchanged.	10
sas Y	52	Skip next instruction if C(AC) is the same as C(Y). C(AC) and C(Y) left unchanged.	10
shift	66	See shift group	5
skp	64	See skip group	5
sub Y	42	Subtract C(Y) from C(AC)	10
xor Y	06	Exclusive OR bits of C(AC) with C(Y)	10

OPERATE GROUP

This is a micro program set of instructions. Thus $cla + cli + clf = 764207$ (5 microsec.)

Instruction	Code	Explanation
cla	760200	clear AC
clf	760001-7	clear selected Program Flag
cli	764000	clear IO
cma	761000	complement AC
hlt	760400	halt
lat	762200	load AC from Test Word switches
stf	760011-7	set selected Program Flag

SKIP GROUP

Skip next instruction if condition is met.

Instruction	Code	Explanation
sma	640400	skip on minus AC
spa	640200	skip on plus AC
spi	642000	skip on plus IO
sza	640100	skip on ZERO (+0) AC
szf	64000f	skip on ZERO flag (f = flag #)
zso	641000	skip on ZERO overflow (and clear overflow)
szs	6400S0	skip on ZERO sense switch (S = switch #)

SHIFT/ROTATE GROUP

Shift is an arithmetic operation. The sign bit is left unchanged and vacated bits are filled with the sign. Rotate is a logical operation and cycles the bits (including sign) in a closed ring. The number of steps is the number of ONE's in bits 9-17 of the instruction (9 max).

Instruction	Code	Explanation
ral	661	rotate AC left
rar	671	rotate AC right
rcl	663	rotate combined AC & IO left
rcr	673	rotate combined AC & IO right
ril	662	rotate IO left
rir	672	rotate IO right
sal	665	shift AC left
sar	675	shift AC right
scl	667	shift combined AC & IO left
scr	677	shift combined AC & IO right
sil	666	shift IO left
sir	676	shift IO right

IN-OUT TRANSFER GROUP

The number of variations in this group may be greatly increased for optional or special in-out equipment.

Instruction	Code	Explanation
ppa	730005	punch paper tape alphanumeric
ppb	730006	punch paper tape binary
rpa	730001	read paper tape alphanumeric
rpb	730002	read paper tape binary
tyi	720004	read typewriter input switches
tyo	730003	type out

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