

**A Semiconductor Packaging
Hardware Donation
To
Semiconductor Equipment and
Materials International**

[Handwritten signature and date]
10/13/07

Submitted by:

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This collection of packaging hardware illustrates the history of packaging technology, beginning in the late 1940s, with the evolution of the simple transistor. In the late 1950s, with the invention of the integrated circuit (IC), technology moved on through the 1960s, with the evolution of sophisticated packaging hardware. Progress continued into the 1970s, with extremely complex packaging hardware. Further sophistication developed through the 1980s and 1990s, and there are several samples of this technology in our collection of hardware.

In all, there are a total of 80 specific donation items numbered 1 through 80. Each of these 80 items consists of a box of hardware containing from 10 to 120 components in each box. Over half of these components are gold plated, and therefore represent a significant value (estimated to be over \$2,000) in precious metal alone. In total, the collection ranges from 4,000 to 5,000 specific package components and piece parts. In addition to these individual components, there are six subsystems displaying components assembled into printed circuit boards. These subsystems include an electronic watch, a computer hard disk drive, a sophisticated power supply, an automotive voltage regulator, an electronic Ricoh camera, a Sharp pocket calculator, and an AST motherboard containing an Intel 486 processor.

The following discussion will begin with item #1 and proceed through to item #80, explaining the contents of each of these hardware boxes.

#1 – This collection of seven parts presents the most ubiquitous package types used over the past half century. These packages protect semiconductor integrated circuits, while facilitating their attachment to the next level of hardware, which is usually a printed circuit board. The original TO (transistor outline) headers were the package of choice throughout the 1950s. These small circular metal rings with up to 12 wire leads, held in place by insulating glass beads, were an outgrowth of simple transistor packages with 3 leads in the same format.

In the late 1950s, IBM developed an integrated circuit with a need for 16 leads, and this led to the next family of packages now known as pin grid arrays (PGAs). Since much of the printed circuit board in use today has circuit traces running parallel, accessing the pins in a pin grid array became a design problem.

In the early 1960s, this led to the development of yet another format known as the flatpak, with leads running in parallel. However, unlike the previous generations of packages, which were all through-hole mounted in the printed circuit board, the flatpak was surface mounted, and this created a whole new set of attachment problems.

In the mid-1960s, this led to the development of the dual inline package (DIP), which offered the simplicity of formerly used through-hole mounting, while still maintaining parallel circuit trace designs. As the DIP packages grew larger, with up to 40 leads, the amount of board space consumed became excessive, and designers searched for yet another package format with a more compact footprint.

This led to the next generation, known as quad packages, with leads on four sides of a square perimeter. The difficulty of circuit design around a four-sided package emerged once again, forcing the use of these packages into multi-layer circuit boards to accommodate the array of pad connections.

Reacting to this problem, semiconductor package producers shrunk the original DIP package, which then emerged as the "mini-DIP." Today, virtually all IC packages are some modification or variation on these five simple packages shown in item #1.

- #2 – Before IC packages were developed for memory circuits in the 1960s, virtually all memory used in computers consisted of magnetic cores (miniature-ferrite "donuts") strung on an XY web as shown in item #2. One of the primary producers of these passive memory systems was FerroxCube Corporation of upstate New York. This was the predecessor of the integrated circuit memory chip.
- #3 – This collection of approximately 300 semiconductor packages represents a more detailed view of the state-of-the-art throughout the 1950s. The TO-16 headers with the small round pedestals were designed to accommodate low power integrated circuits. On the other hand, large power transistor chips required effective heat dissipation, so massive copper slugs were developed into diamond-shaped packages as shown in the collection, for dissipating heat from such power chips. Even beryllium oxide, an expensive white ceramic with very high thermal conductivity, was incorporated into some of these packages to isolate the chip from the copper base, which was grounded to the chassis. Most of these packages were sealed with a metal can, which was welded to the copper flange to create a hermetic package.

In the right hand corner of this box there is a 1 1/4-inch silicon wafer mounted vertically between the styrofoam and the box wall. This was the traditional wafer size used during the early 1960s.

- #4 – This represents a more intense collection of TO-3 and TO-66 power packages, manufactured from copper metal (stamped flanges) and plated with nickel (and occasionally gold).
- #5, #6 – These are small silicon transistor and integrated circuit chips, from the early 1960s, used for low power applications.
- #7, #8 – These are large integrated circuit chips produced by Fairchild Semiconductor during the late 1960s, for advanced circuit design. The chips are enclosed in stacks of small plastic trays with square cavities, known as “waffle paks.”
- #9, #10 – This is a double sided box with samples on both sides. Side #9 shows another 1 1/4-inch wafer (like that in Box #3), and a 2 1/4-inch wafer. Along with these wafers there are a series of small 3-lead transistor packages and a collection of seven flatpaks designed with ceramic substrates attached to metal stamped leadframes. Also included is an early version of one dual inline package (DIP) prior to lead separation and encapsulation.

Item #10 shows a collection of ceramic substrates that have been processed with different pattern configurations. Most of these package parts are the base, upon which the integrated circuit is mounted. In most cases, these bases require a cavity. Not shown here is the ceramic cap, which is placed over top of the base and leadframe combination, in traditional dual inline package configurations.

The black metallization pattern seen on the base of these package parts, often overplated with gold, was deposited on the ceramic by a process known as “screen printing.” The metal pattern begins as a paste consisting of molybdenum and manganese powder, which is then screen printed onto the ceramic surface and fired in a hydrogen furnace at a temperature of 1500-1700°C to sinter the paste particles together, forming a continuous electrical conductor.

After gold plating this pattern, the silicon chip is attached to the gold plate with a gold-silicon eutectic material, which is a conductive metallic low melting “glue.” Virtually all of these ceramic piece parts were made from sintered 94% aluminum oxide, except for the beryllium oxide power flange (diamond-shaped) shown in the upper right corner.

In the late 1960s, memory integrated circuits were developed that could be erased using a blast of ultraviolet (UV) light through a transparent window on the top of the package. One of these windows, made from clear sapphire, is also shown in this collection.

Metal lids were often attached to these ceramic packages using a gold-tin low melting alloy stamped into the shape of a preform that looked like a metal window. This is also shown in the collection. In other cases, a low melting glass preform was used to seal certain packages, and this is shown in the green glass examples.

#11, #12 – In the late 1960s, IC chips became much more sophisticated, requiring greater numbers of leads to connect these chips to the printed circuit board. Box #11 shows 25 different packages used by Fairchild Semiconductor in this time frame, including a 36-lead DIP and a 36-lead flatpak, with wire pins emerging from glass-metal seals through opposite sides of the package.

Box #12 shows an extreme extension of flatpak technology using a glass metal seal. The largest of these three packages is 50-leads, with full gold plating on each package. Next to these is a 2-inch square ceramic white substrate designed to accommodate nine different chips in one of the earliest multichip memory arrays.

Also shown in this display is a piece of tantalum foil used in manufacturing tantalum capacitors. And the dual inline pattern shown on the pink opaque ceramic was screen printed by a company in England, known as Letraset. This moly-manganese paste was screen printed using high speed processing onto a releasable adhesive tape.

#13 – This is the roll of tape that was used to metallize dual inline ceramic package bases at a very high speed using reel-to-reel tape-transfer processing. Aimed at cost reduction, this process was invented and patented under Fairchild jurisdiction by Dan Rose.

#14 – This collection: a dual inline package, a four-sided quad package, and two power transistor packages manufactured on beryllium oxide substrates, was manufactured by Coors Ceramics. Many other companies in the 1960s manufactured similar products, including American Lava, Metceram, Kyoto Ceramic and NGK Spark Plug to name a few.

#15 – Manufacturers of glass-metal seal packages were also graduating into larger and larger formats as shown in this collection from Bendix Micropackaging, featuring a 32-lead package.

#16 – By the end of the 1960s, a vast collection of metallized ceramic packages were being offered by many companies. These packages were configured as dual inline packages with up to 50-leads, and four-sided quad packages with similar quantities of leads. Most of these packages were gold plated, and the metal lids that were attached to the packages after IC chip mounting, were also metal with gold plating. In short, the precious metal costs in these packages reached astronomical levels, so that recycling of old reject devices was a necessity.

Recovery of gold throughout the 1960s by semiconductor companies was a major operation. The sequence of reclaim operations necessary to recover

- the gold and reuse a ceramic package is shown in this collection. The precious metal value alone of the 60 different IC packages and seal lids in Box #16 is estimated at over \$300.
- #17 – This strip of dual inline packages (DIPs) with gold plated leads illustrates a new trend in packaging that began in the late 1960s, known as “flip-chip packaging.” The concept behind this package format was to eliminate the traditional wire bonding that connected the chip to the package. In this case, a precision metallized pattern was screen printed onto the white ceramic substrate, so that the integrated circuit chip could be mounted face down directly to the metallized traces. Bumps were created on the chip bonding pads to match the tips of these traces, and create a compression bond connection.
- #18 – Recognizing the gain in productivity that IC companies achieved from continuous strip operation in assembling dual inline packages, the package manufacturers themselves also began to incorporate strip line processing.
- #19 – Facilitating much of this automated processing were connector manufacturers such as AMP Incorporated, who provided sockets, DIP handling equipment, and connectors.
- #20 – DIPs continued to flourish as the package of choice for low cost automated printed circuit board assembly throughout the late 1960s and into the 1970s. This created a vast number of variations including a wide variety of ceramics, plating choices, and leadframe configurations. The 80 different packages in Box #20 shows some of these variations.
- #21 – In 1968, Fairchild Semiconductor became concerned about the proliferation of endless packaging formats used by different systems manufacturers, and commissioned a competitive analysis of what primary packaging system was being used by various electronic system providers. The 42 different color photos shown on the seven pages of this collection represent the state-of-the-art in 1968 used by IBM, Honeywell, Delco, Polaroid, General Electric, Motorola, Philips, RCA, Siemens, NEC, and Toshiba. Competitive analysis was also performed showing Fairchild’s packaging approaches versus Motorola, Signetics, TI, and National Semiconductor. For small pin count configurations (under 40-leads), the dual inline package continued to prevail. For larger formats, however, (greater than 50-leads) the quad flatpak had emerged as the format of choice.
- #22 – Stamped DIP package parts were being produced by the hundreds of millions and stamped leadframes were the very high volume product. This box contains 2000 stamped DIP leadframes in 16-lead format made from a nickel-iron alloy (42-alloy).
- #23 – In order to move these dual inline frame strips through very high speed assembly operations, sophisticated DIP cassette carriers were used for high speed strip loading and unloading. This shows the cassette used for flat leadframes..

- #24 – In contrast, leadframes were often shipped in the preformed U-shaped configuration as shown in item #24. This sample carrier from Mech-El Industries shows how frames can be handled when they are preformed.
- #25 – This box contains 18 different leadframe styles, represented by 50 strips altogether, and each leadframe pattern illustrates a different design and approach. Some of the leadframes are etched or stamped, some are pre-molded into packages, others have been post-molded after the device has been die attached and wire-bonded to the frame. The list of leadframe types illustrated is on the top page of the stack in the box.
- #26 – This is a typical plastic shipping tube for shipping finished dual inline packages in between final operations or to the final customer. This tube contains eight 40-lead dual inline packages constructed in the CERDIP configuration (ceramic lid and base with stamped 42-alloy leadframe).
- #27 – This collection consists of five DIP shipping tubes, each tube containing 15 24-lead DIPs. Note that some of these DIP packages have transparent sapphire windows on the top of the package so that the UV (ultraviolet) erasable chips in the package can be reprogrammed after flashing light through the transparent window.
- #28 – This is a typical semiconductor logic board out of a Burroughs computer of the vintage 1965. The dual inline package was just gaining in popularity at that point and began to reach large volume production.
- #29 – In order to achieve significant cost reduction, materials engineers everywhere were looking for alternate ways of manufacturing integrated circuit packages. This approach came from Erie Ceramic Arts, and effectively utilized the same technology as is used in manufacturing the chassis of washing machines and dryers. The technology uses rigid steel plate with an overcoat of porcelain. The porcelain is then screen-printed with a metallized paste, and sintered to create patterns on the surface of the porcelain insulation. The underlying metal can then be used for chip mounting. Several attempts at using this technology were made during the late 1960s, but the weight factor, and imperfect surfaces of the porcelainized steel could only be used for non-critical thick film circuitry on panels where weight was not an undesirable feature.
- #30 – This is an Atari game cartridge of the early 1970s, demonstrating the growing importance of direct chip-on-PC board packaging. The cartridge was manufactured by Advanced Micro Devices.
- #31 – In the late 1960s, Diacon introduced a high density CERDIP with leadframe spacing at twice the density of standard 100 mil DIP pin spacing. The package was already pre-assembled and the only user function was die attach and wire bond followed by cap seal and plating.

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- #32, #33 – Toward the end of the 1960s, some companies were experimenting with multichip array packages, which could act as memory modules. Box #32 contains many of these modules, which typically housed anywhere from 8 to 12 integrated circuit chips, mounted on very fine line patterns, mostly in quad pak configurations with through-hole mounting into their printed circuit board. The metallization patterns on these packages pushed the limits of screen printing technology to the point where etched thin film circuits were often used to achieve super fine-line geometries.
- #33 – This assembly of surface mounted flatpaks shows the wide variation in size, pin count, and package configuration.
- #34 – In the late 1960s and early 70s, multichip modules such as those shown in this box became popular. These were miniature circuit boards, executed on ceramic or plastic, with several fully packaged chips, along with discrete components comprising the modules. Such complex packages were frequently used for memory array modules, and in some cases, full system configurations.
- #35 – Texas Instruments was a notable standout in developing these complex modules, utilizing many different components. This unit illustrates the complexity of their inner circuits.
- #36, #37 – The centerpiece of this group is one of the first multichip memory modules ever built, with 16 different chips mounted in one square inch quad flatpak. Also shown is an extremely fine line, etched geometry pattern, for a 250-pin chip. Other quad pak configurations are shown on the opposite side of the box, as quad packages became the package of choice for very complex, high pin count devices.
- #38 – This is another eight chip memory module, alongside a complex dual inline package used for hybrid circuits. Such circuits were often built on a flat ceramic insert, that was seated in the large cavity of this DIP package.
- #39 – As very high circuit density progressed, the geometries became smaller, and super fine-line circuitry on ceramic, as shown on this substrate, was carefully executed by such companies as Cirqon Technologies.
- #40, #41 – At the same time that silicon technology was progressing through the 1960s and into the 1970s, gallium arsenide semiconductor technology was also advancing, as shown by these solid-state numerical digits. These 14 segment LED (light emitting diode) displays were manufactured by Monsanto, and widely used in solid state numerical presentations.
- #42 – Other attempts at larger LED displays are shown in this collection of numerical digits and individual light emitting diodes.
- #43 – These packages illustrate a different approach by Monsanto, to manufacturing seven-segment displays using less LED material, by creating

- reflective surfaces inside each segment to spread the light. These became popular for printed circuit board displays.
- #44 – Following the successful development of silicone-molded dual inline packages by Signetics in the late 1960s, other companies began experimenting with cheaper epoxy-molded packages in the early 1970s, and this created a major transition away from ceramic packages, and into plastic dual inline packages. Following the earlier ceramic technology, these plastic DIP packages were often configured as pre-molded DIPs, containing die attach pads and gold plated leadframe tips. Eventually, other companies, led by National Semiconductor, began manufacturing epoxy molded dual inline packages as post-molded configurations in the early 1970s.
 - #45 – The rapid escalation of pin counts in packages during the 1970s created a windfall of business for connector manufacturers, who were stamping out enormous quantities of pins as shown in this item. Such companies as Berg and AMP were busily supplying the semiconductor industry with more and more product.
 - #46 – This collection of ceramic chip carriers and quad flatpaks illustrates the startling improvement in density, using thick film manufacturing techniques to produce very small packages with tight tolerances on circuit traces.
 - #47 – Modular technology, using these chip carriers, became a popular method of producing subsystems, such as those shown in this box.
 - #48 – These samples of a 28-pin and 48-pin chip carrier were used in the Motorola pocket pager of the mid-1970s. Such ceramic chip carrier technology was spreading to other systems quickly.
 - #49, #50 – Pre-molded plastic quad paks also gained in popularity, as a cheaper replacement for their ceramic counterparts, as illustrated in these two items.
 - #51 – Not to be outdone, the ceramic chip carrier manufacturers began to increase the complexity of their products, as shown in the 50 different samples in this collection.
 - #52, #53 – Another technology that became popular in the 1970s was the concept of socketing ceramic quad flat paks, and molded plastic quad paks, so that these individual chips could be removed and reprogrammed as necessary. Several configurations of this package type are illustrated in items #52 and #53. Most of these samples of sockets and quad paks were manufactured by AMP Incorporated, one of the largest connector manufacturers.
 - #54 – This is a typical strip of pre-molded quad paks from AMP.
 - #55 – GTE also began producing socketable quad paks, shown in this collection.

- #56 – Such quad paks began to generate enormous amounts of heat, requiring elaborate heat sinking methods, shown in this collection. In the 1970s, tighter pin spacing and higher pin counts began to invade the quad market, as it had earlier invaded the dual inline and prior package configurations in the 1960s.
- #57, #58 – Meanwhile, greater pin density and higher heat dissipation led to exotic types of packages as seen in this collection of 35 samples.
- #59 – Not to be left out, manufacturers of flexible printed circuit tape began flooding the market with super-fine-line geometries, executed on reel-to-reel tape patterns, as shown in this collection from some 40 different suppliers. The reel-to-reel tape assembly process for packaging chips took a huge turn upward in the 1970s, when National Semiconductor launched its TAB (tape automated bonding) program with 3M Corporation, in developing a fully automated gang bonding process. Samples of this are shown in this collection.
- #60 – During the early 1970s, solid state watch modules began to appear, as shown in this array. Such modules were initially directed at the emerging LED watch market, which used single chips to present each of the 4-digit displays. As time progressed however, the industry switched away from LED watches in the mid-1970s, with the introduction of liquid crystal displays, as shown in item #61.
- #61 – This is a watch chassis, strap, and finished watch from Fairchild Semiconductor, manufactured in the late 1970s, when liquid crystal watches were gaining in popularity over the power-hungry LED watches.
- #62 – By the early 1980s, the level of sophistication in packaging had reached incredible densities, as shown in this collection of high-pin-count modules from various suppliers. Of particular interest is the logic and processor packages from Intel, which dissipate so much heat that enormous copper heat sinks are required on the backside of the 244-pin ceramic package. Pin spacing has decreased to incredibly small dimensions, and every package in this collection shows leading edge technology.
- #63 – This single super-high density package frame from Olin Interconnect technologies clearly reveals the incredible density of wiring achieved in the 1980s and 1990s.
- #64 – This collection of high power packages, including beryllium oxide power platforms, along with super-high-density quad paks, mounted on copper pillars, clearly reveals the thermal issue. Even simple plastic 14-lead DIP packages have huge heat sinks emanating from the top and the sides to help dissipate power.
- #65 – This is a very high density testing board for a large package, containing 160-pins at the center point.

- #66 – Manufacturers of flexible printed circuitry began honing their skills at super-fine-line geometries, as illustrated in these connector straps.
- #67 – 3M became one of the acknowledged leaders in providing this super-high-density tape for semiconductor applications, and was also the primary provider to National's introductory program. Some different examples of 3M products are shown in this collection, along with 3M photographs of close-ups of their pin configurations at the bonding tips. The concept of so-called "gang bonding," developed by National, then became routine throughout the world.
- #68 – Even Beckman Instruments began adopting super-fine technologies on their chips, to achieve better performance for their trimming potentiometers.
- #69 – This is a computer hard drive from the 1980s, showing circuitry that is primarily executed in quad paks and high density dual inline packages.
- #70 – Such hard drives typically utilize miniature devices that detect magnetic signals, called sliders. Such sliders were manufactured by National Micronetics, and others, as illustrated here.
- #71 – This is a power supply manufactured by Astec, utilizing several power transistors and condensers to achieve smooth solid state performance.
- #72 – This is the interior workings of a Ricoh electronic camera, showing all of the different components wired together, including the master circuitry, which is executed on flexible printed circuit technology. The entire camera is operated by a single major chip, shown as a dual inline high density package. Other items in this collection include a pocket calculator, showing its inner workings, and smart cards developed for the European telephone market.
- #73 – This is a voltage regulator module from a 1985 Mercedes Benz, showing several integrated circuits from National Semiconductor and Motorola. One of these circuits was traced to be the failure point of the module.
- #74 – This is a motherboard from an AST computer of the late 1990s. The startling revelation from looking at these semiconductor packages is the incredibly tight pin spacing. The logic circuits from Cirrus Logic and VLSI Logic, along with the Intel 486 processor, reveals 50 mil pin spacing around all of the quad flat paks and dual inline packages. Such spacing would have been unthinkable in the 1960s, but is now common throughout the latest chip packages.
- #75 – This collection shows a number of test sockets and frames commonly used for evaluating finished integrated circuits.
- #76, 77 – As power dissipation increased dramatically on semiconductor products during the 1980s, complex heat sinks were developed, which required

spring-loaded pressurized contact to dissipate all of the heat generated by the chips. Such dissipation mechanisms are shown in these samples.

#78 – This is a 3-inch fully patterned integrated circuit wafer, that reached its peak of popularity in 1975.

#79 – Here are some samples of earlier silicon boules and crystals, from which wafers have been sliced. These are early 1960 vintage, when 3/4-inch and 1 1/4-inch wafers were popular.

#80 – This is a spool of pure gold bonding wire, that is used to bond integrated circuit chips to packages. Such wire is only one-thousandth of an inch in diameter and is very expensive.

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From: "David Laws" <laws@computerhistory.org>
To: <roseassociates@sbcglobal.net>
Cc: "Dag Spicer" <spicer@computerhistory.org>
Sent: Tuesday, October 09, 2007 9:17 PM
Subject: Pakaging Collection

Dear Dan,

SEMI has transferred your packaging collection to the Computer History Museum. Thank you for the time and effort you put into assembling this extraordinary history of packaging at Fairchild and beyond. We are currently in the process of cataloging the items. We note that you carefully numbered each box. Do you have a record of the contents of each box as identified by these numebrs?

If you do, we would certainly appreciate receiving a copy.

Enclosed

Thank you.

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